

Fig. 1A

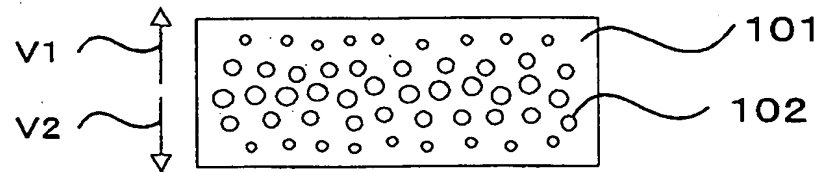


Fig. 1B

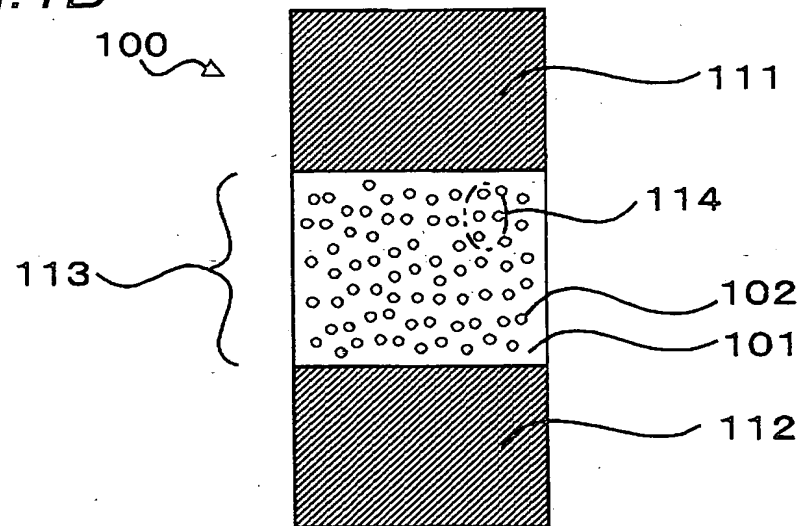
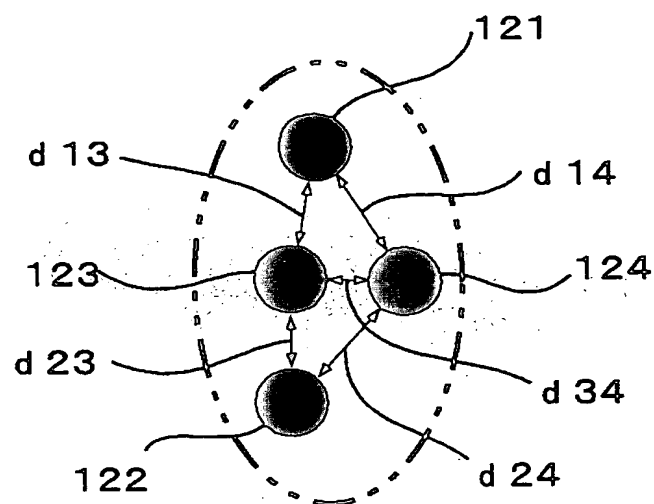


Fig. 1C



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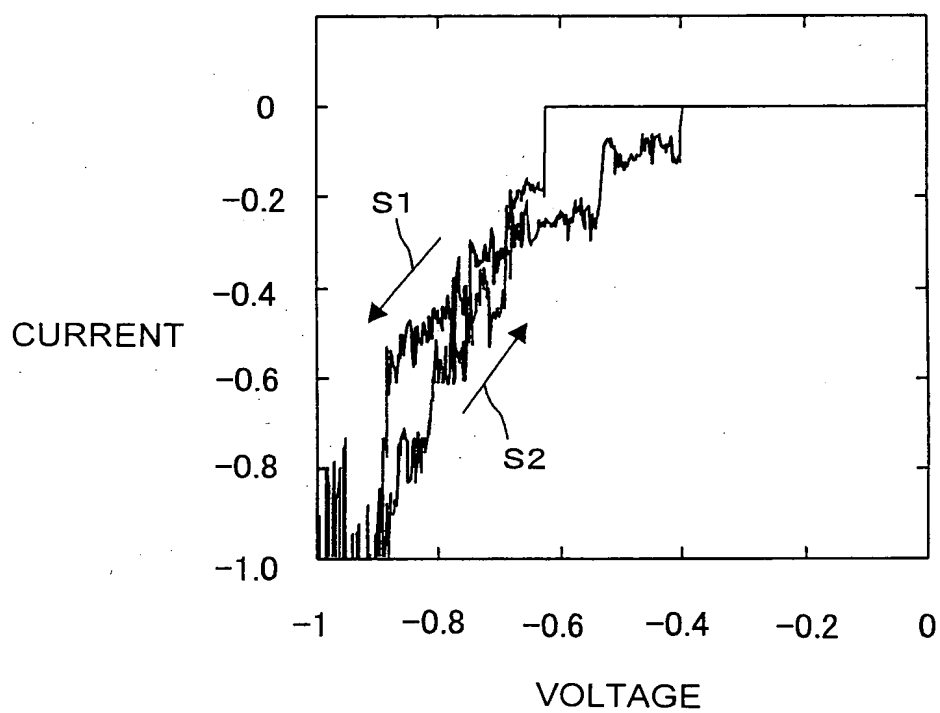
*Fig.2*

Fig. 3A

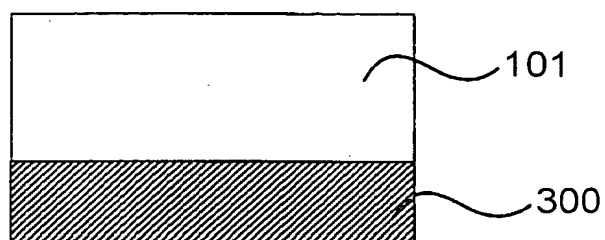


Fig. 3B

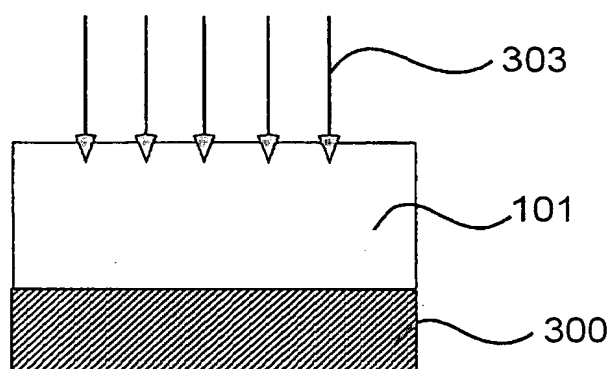


Fig. 3C

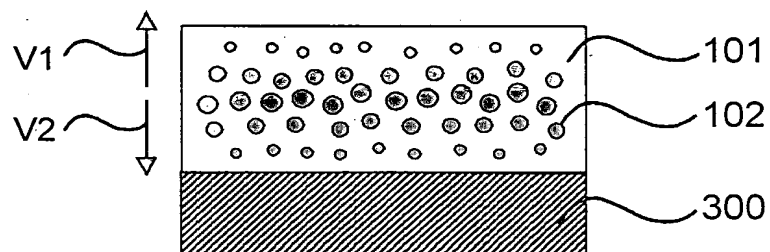


Fig. 3D

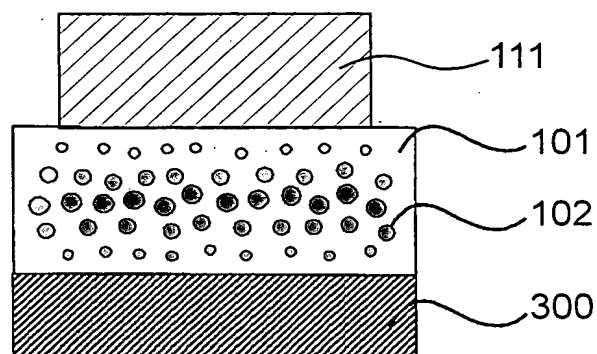
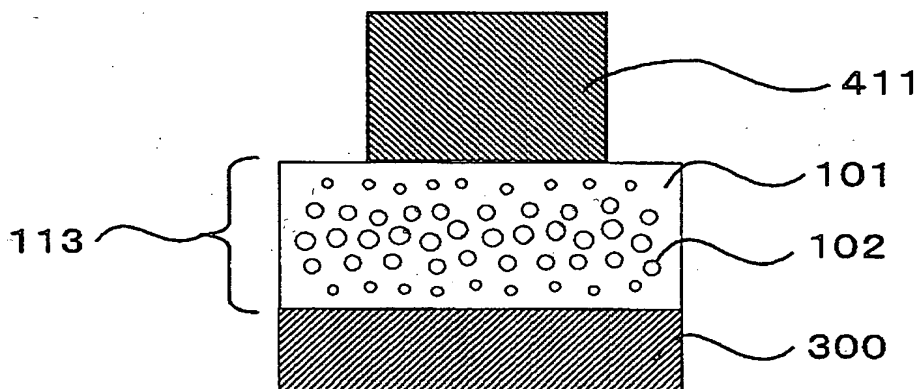
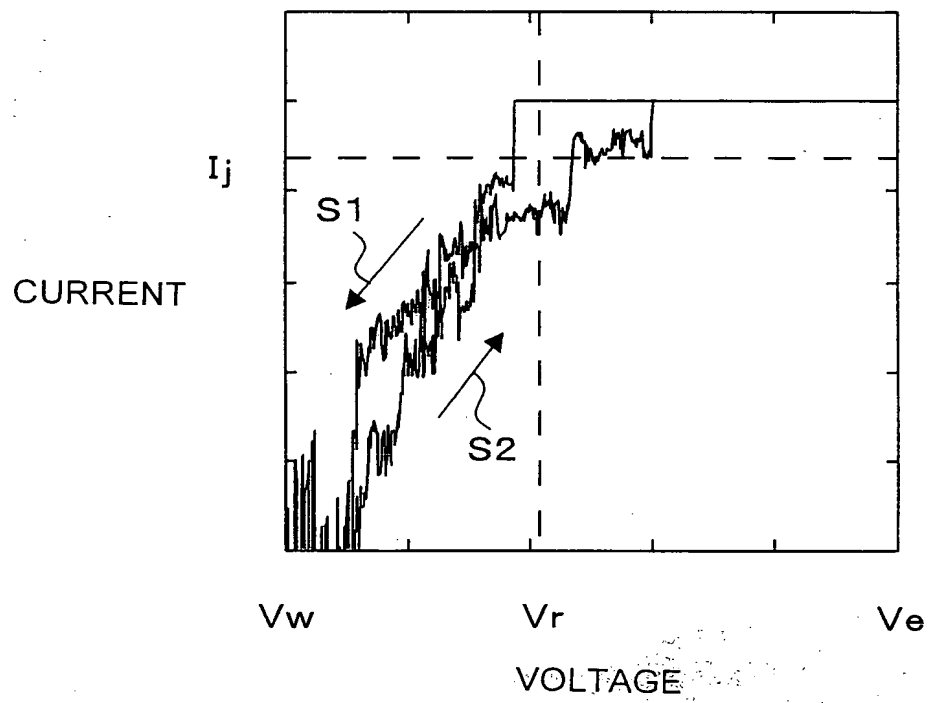


Fig. 4



*Fig.5*

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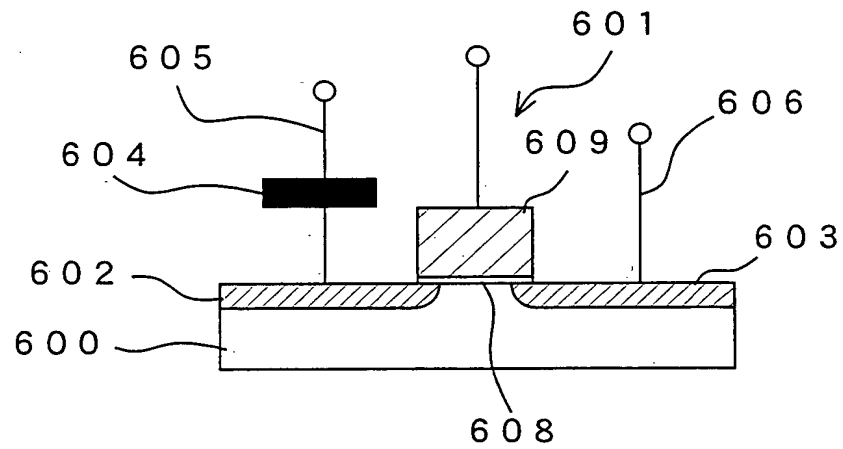
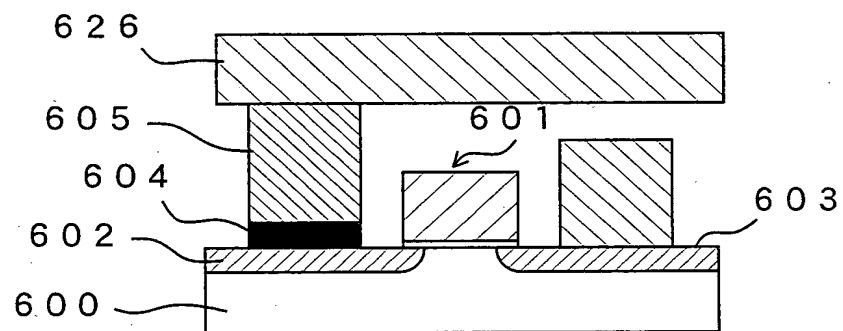
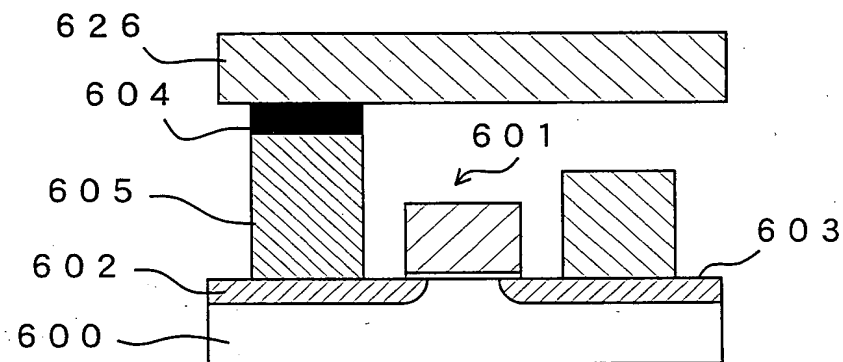
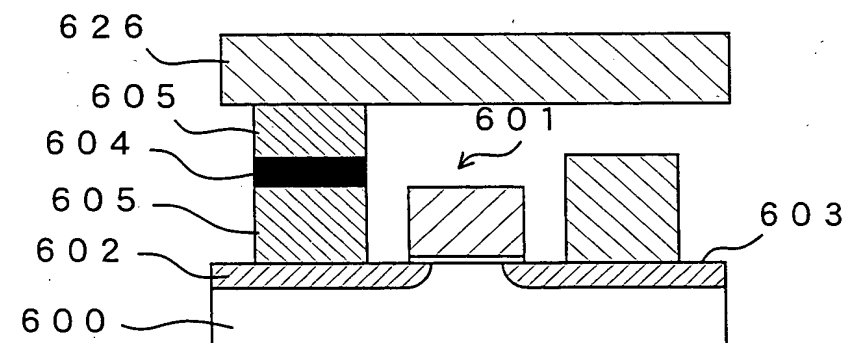
*Fig. 6A**Fig. 6B**Fig. 6C**Fig. 6D*

Fig. 7

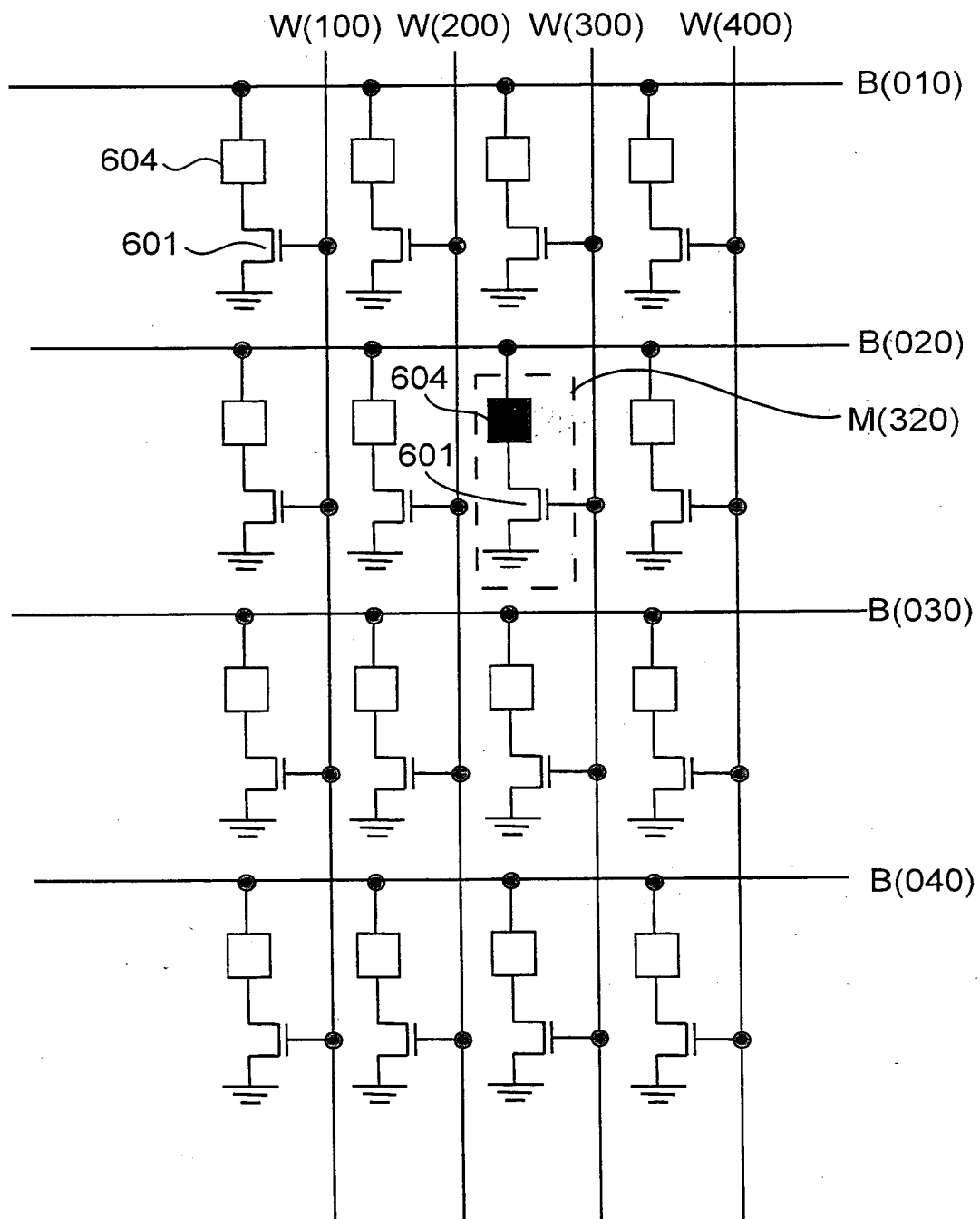
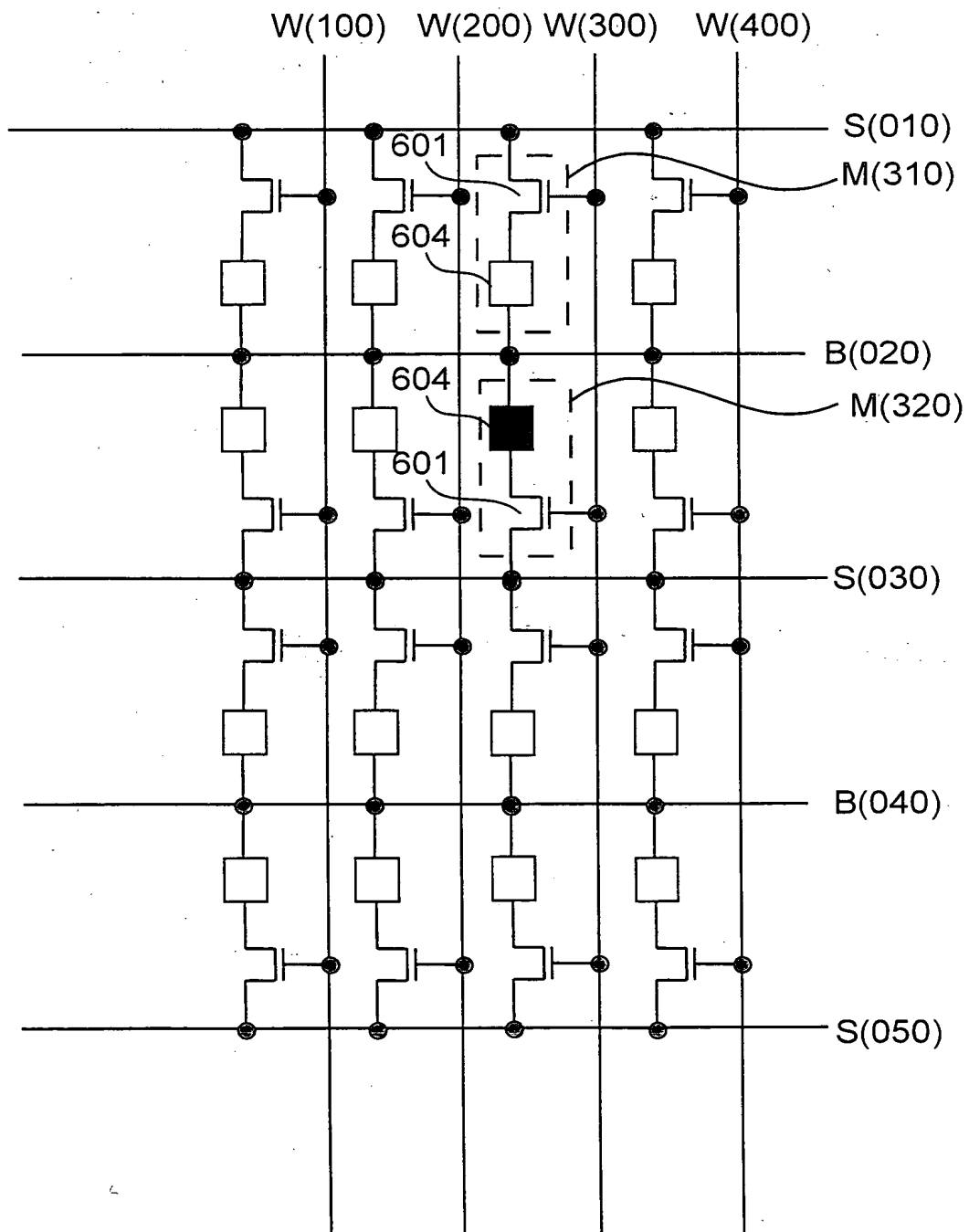


Fig. 8



This cross-sectional view shows a semiconductor device with three memory regions labeled M1, M2, and M3. The device is built on a substrate 900. A gate stack 926 is positioned above the substrate. Below the gate stack, there are several conductive layers and contacts. In region M1, there is a contact 901, a conductive layer 909, and a conductive layer 902. In region M2, there is a contact 901, a conductive layer 903, and a conductive layer 907. In region M3, there is a contact 901, a conductive layer 903, and a conductive layer 908. The substrate 900 has a layer 904 on its top surface, which is patterned into regions 903 and 904. The conductive layers 901, 902, 903, and 904 are shown with different hatching patterns to distinguish them.

Fig. 9B is a cross-sectional view of a device structure. It shows a substrate 900 with a series of raised regions 903. A layer 901 is deposited over these regions, with openings 905 in the layer 901. A top layer 926 is shown above the structure.

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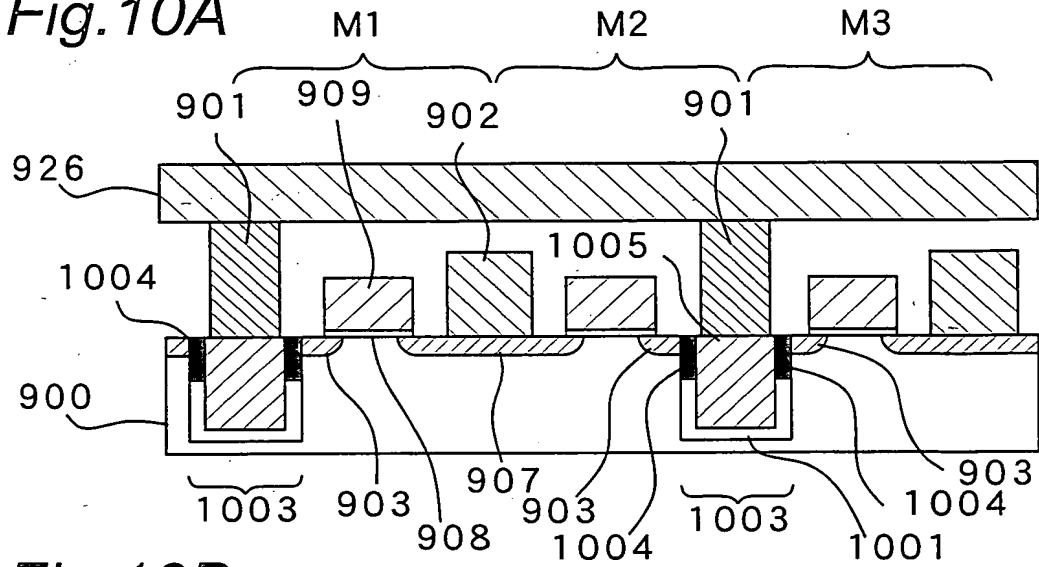
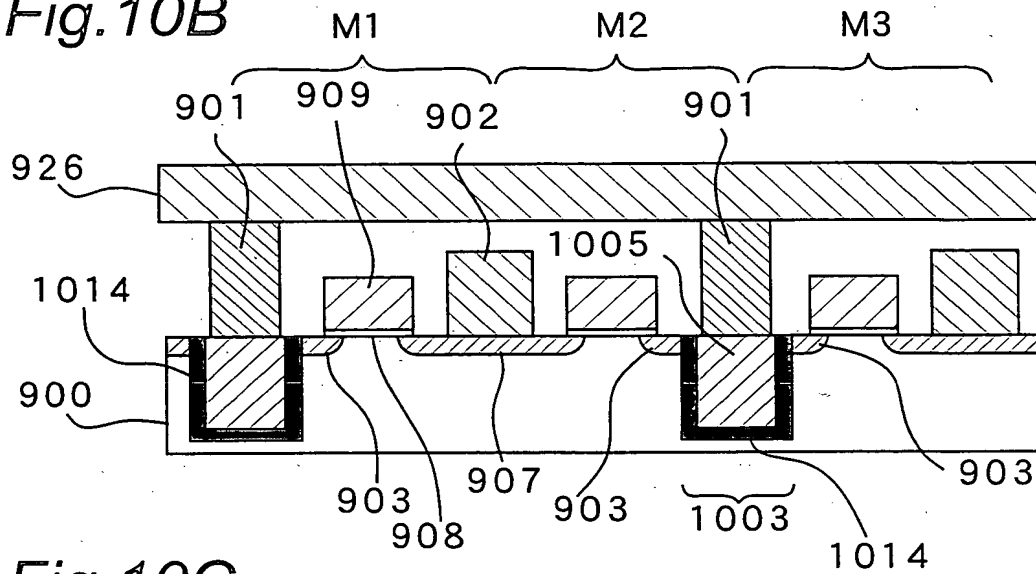
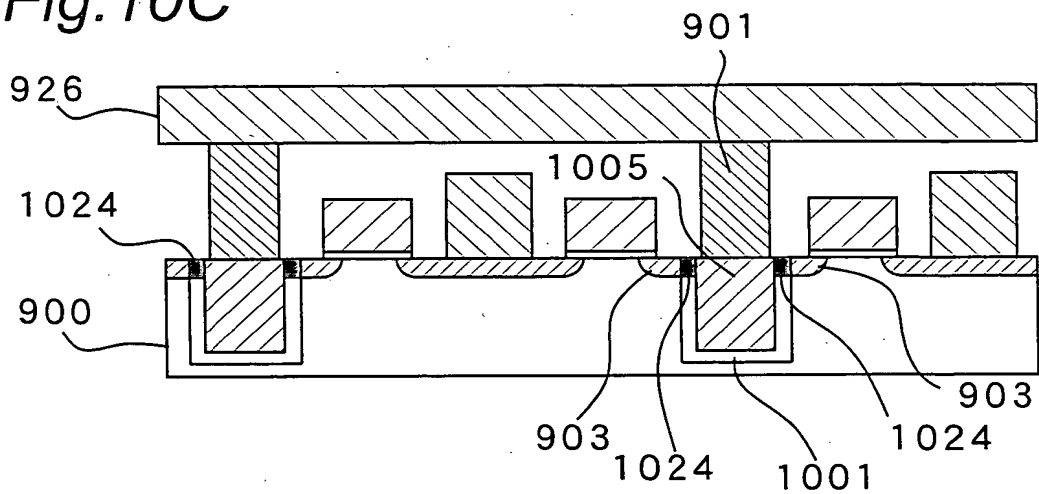
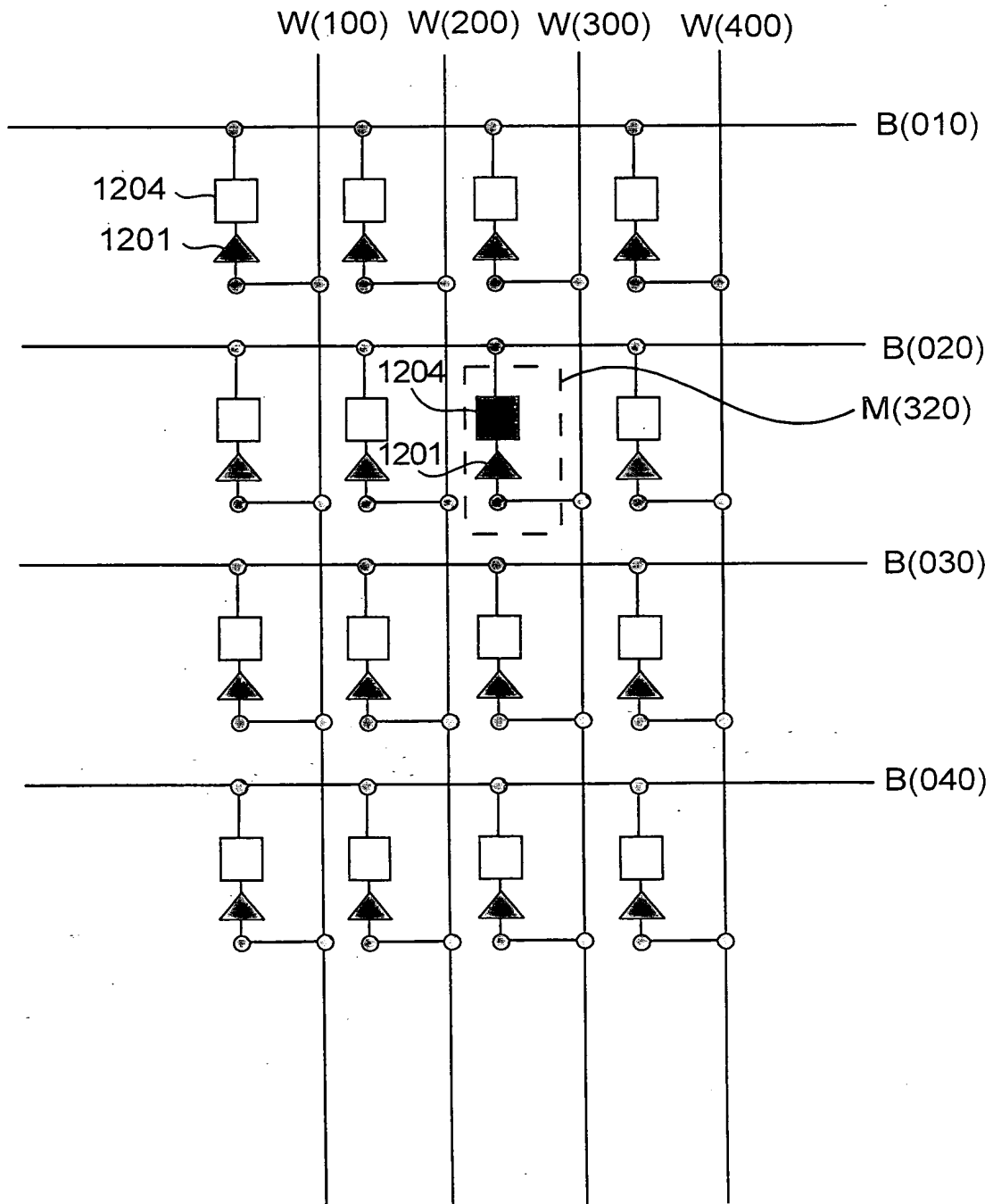
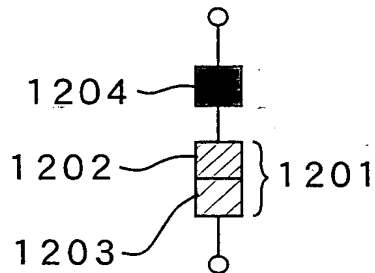
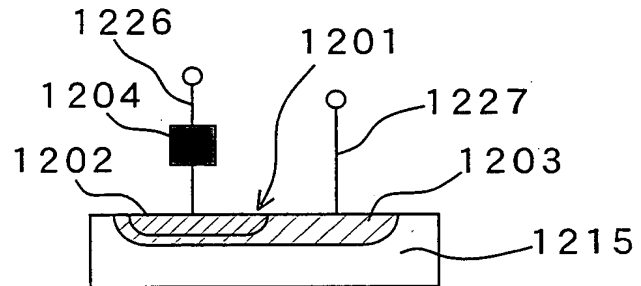
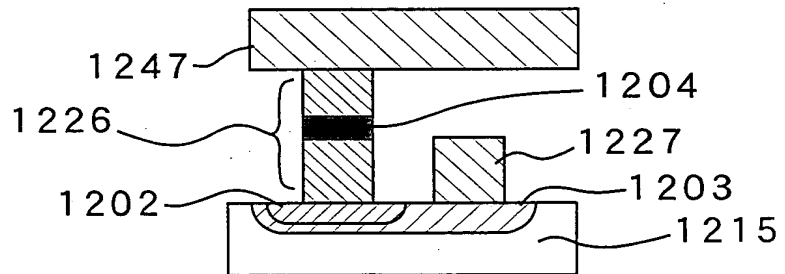
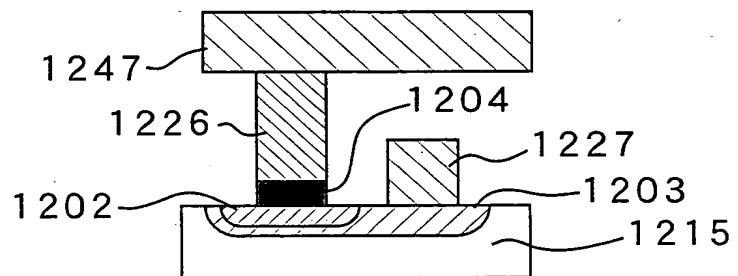
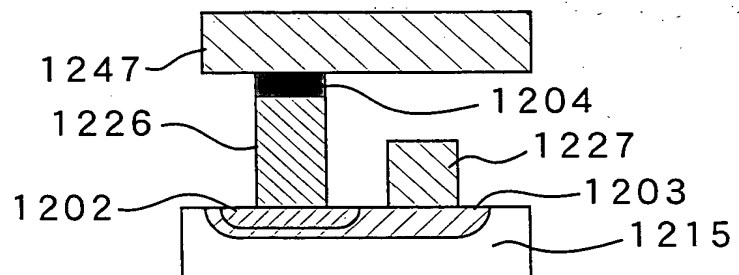
*Fig. 10A**Fig. 10B**Fig. 10C*

Fig. 11



*Fig. 12A**Fig. 12B**Fig. 12C**Fig. 12D**Fig. 12E*

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Fig. 13A

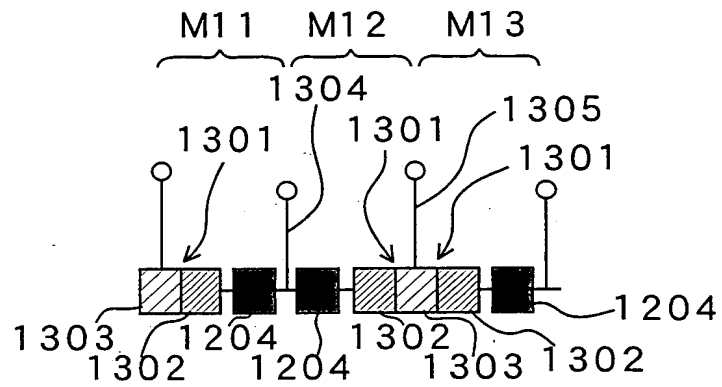


Fig. 13B

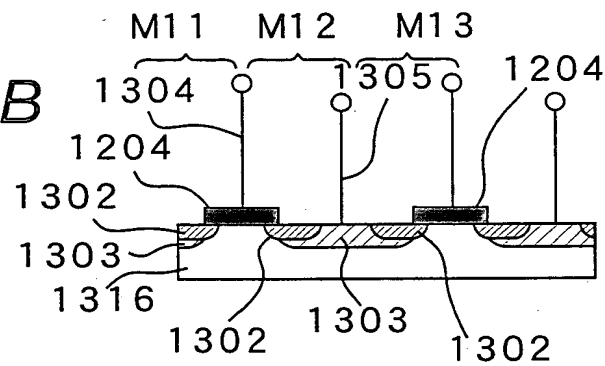


Fig. 13C

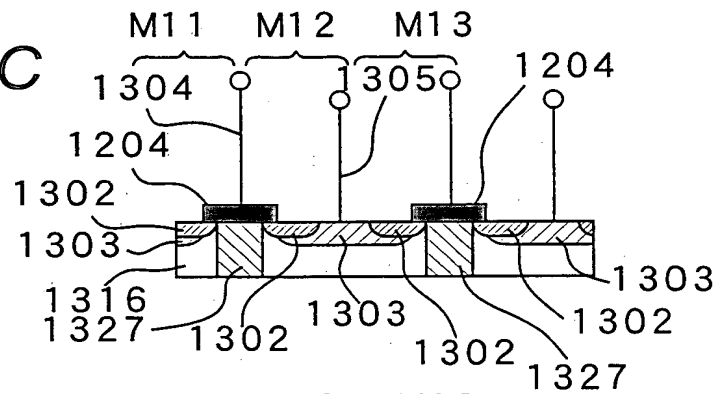


Fig. 13D

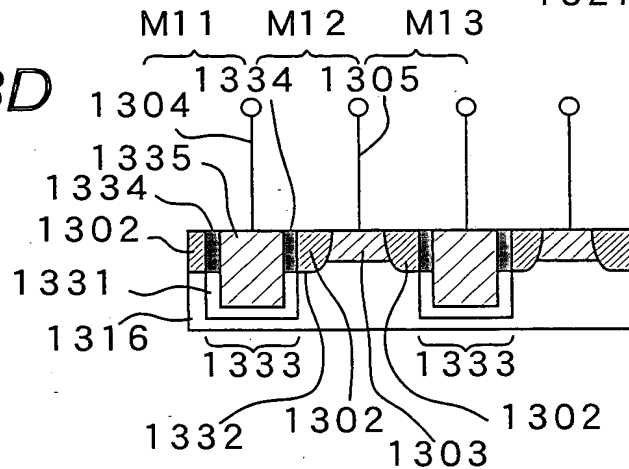
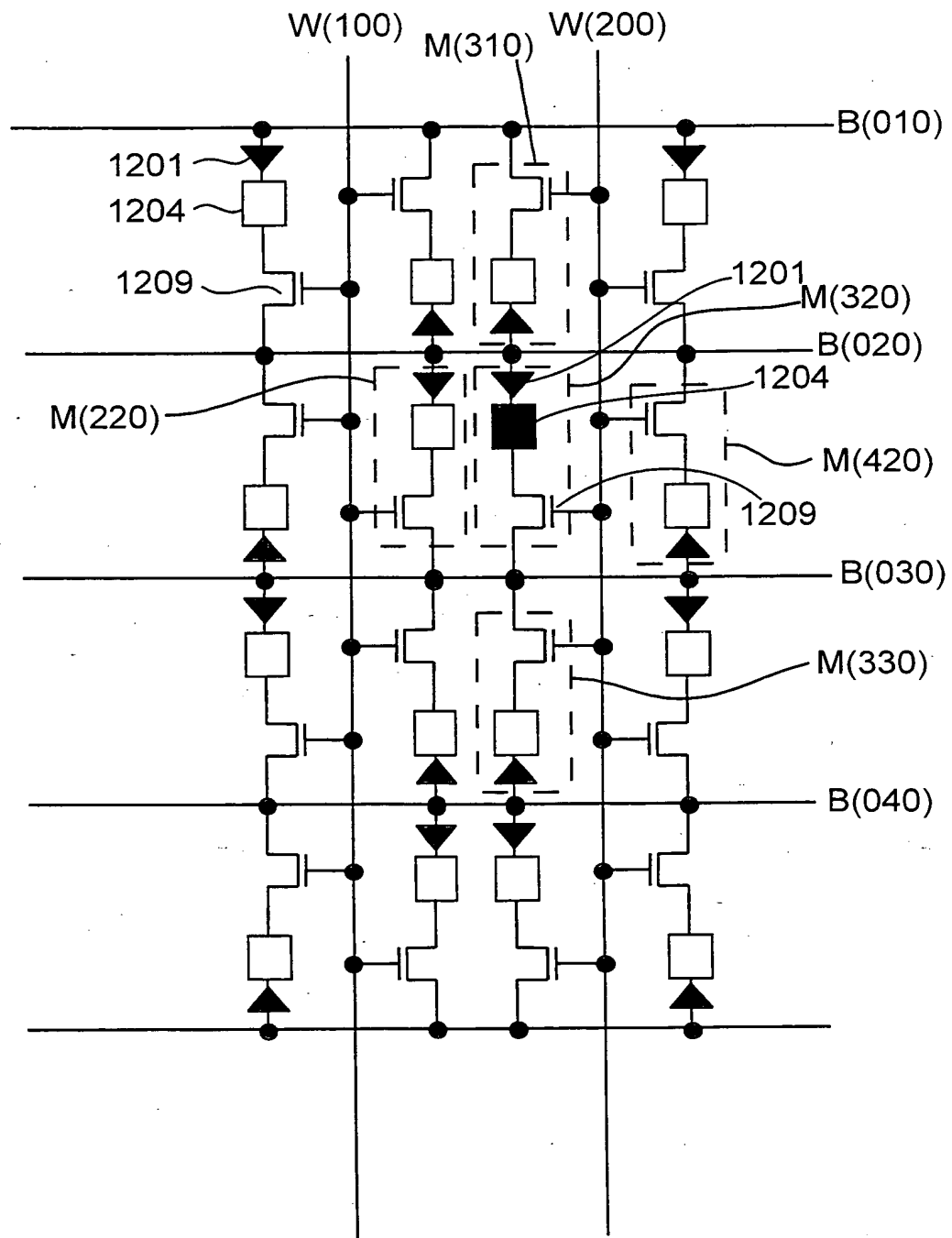
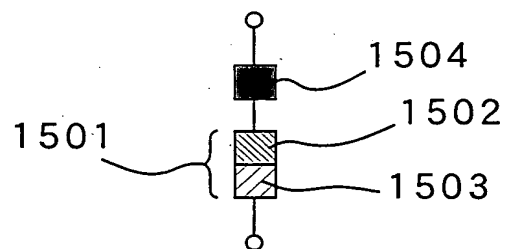
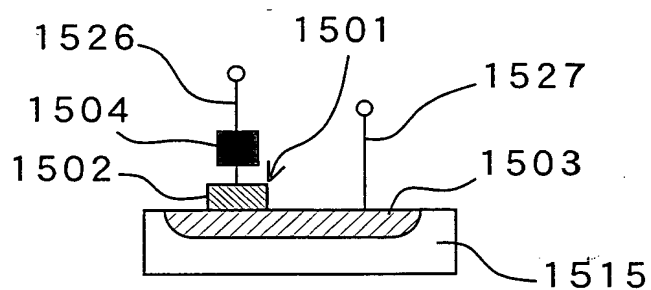
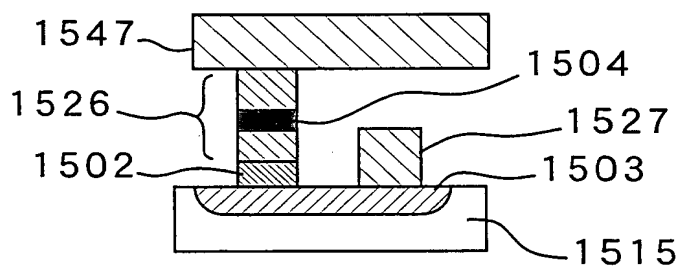
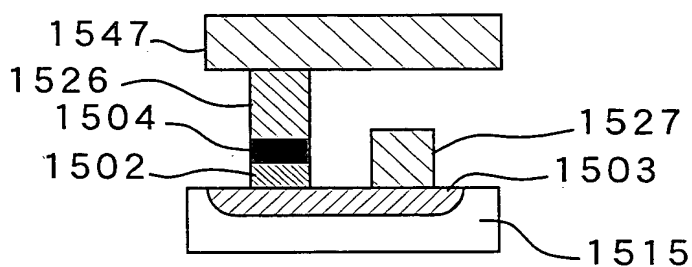
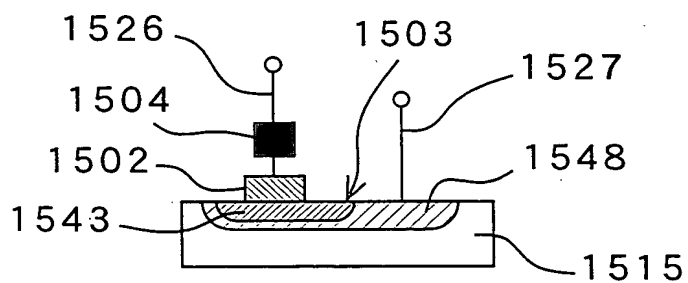


Fig. 14

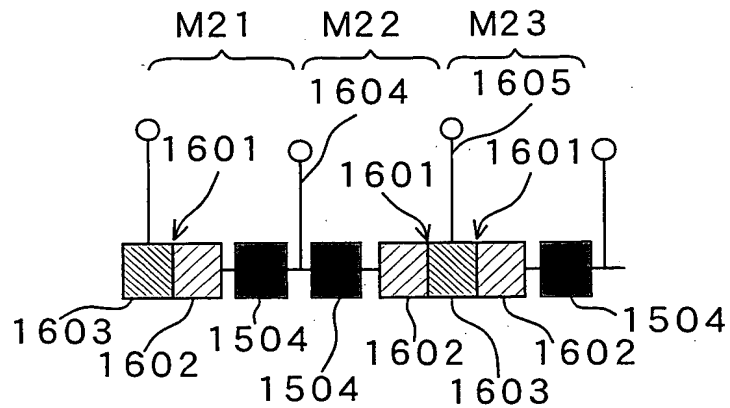


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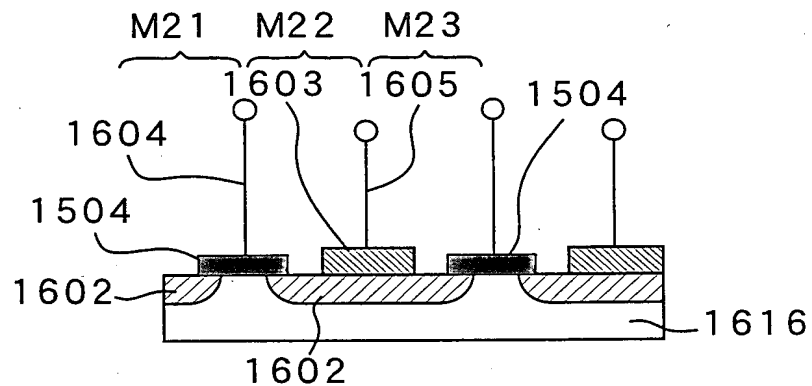
*Fig. 15A**Fig. 15B**Fig. 15C**Fig. 15D**Fig. 15E*

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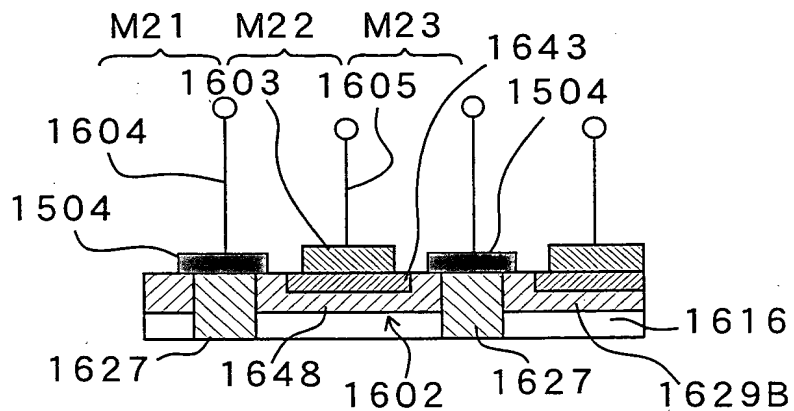
*Fig. 16A*



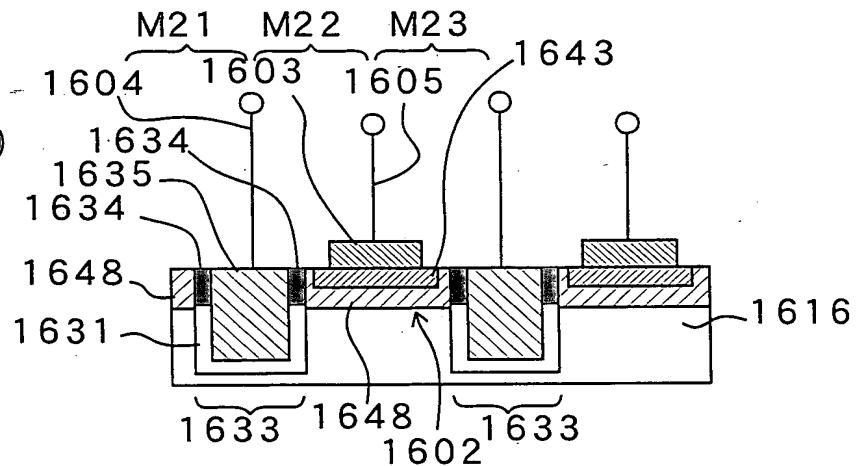
*Fig. 16B*



*Fig. 16C*



*Fig. 16D*



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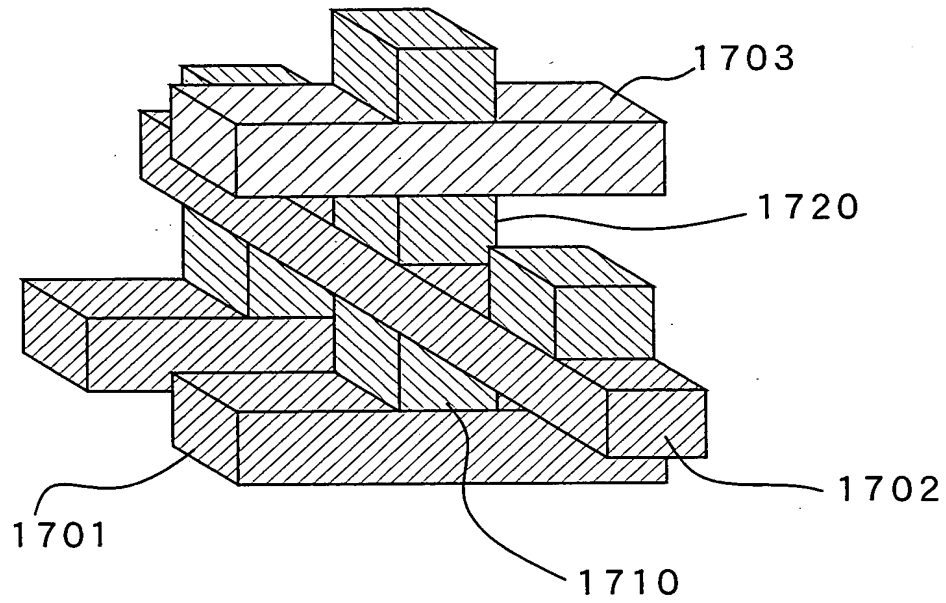
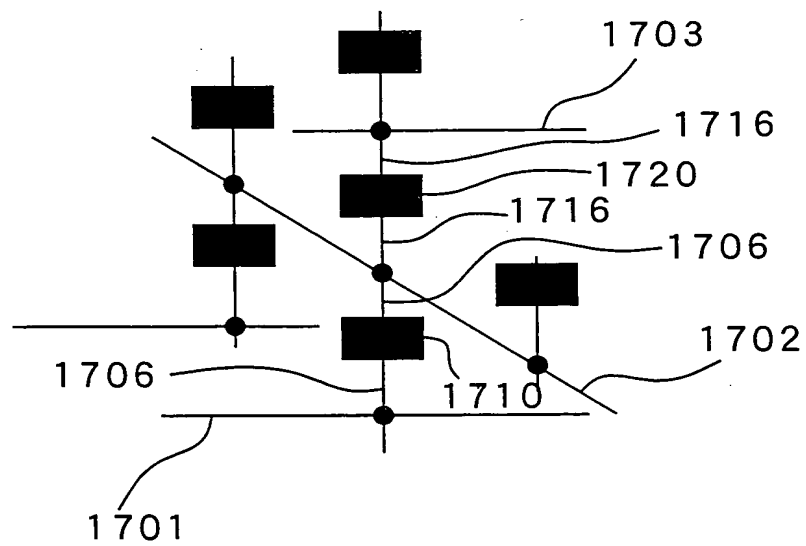
*Fig. 17A**Fig. 17B*

Fig. 18A

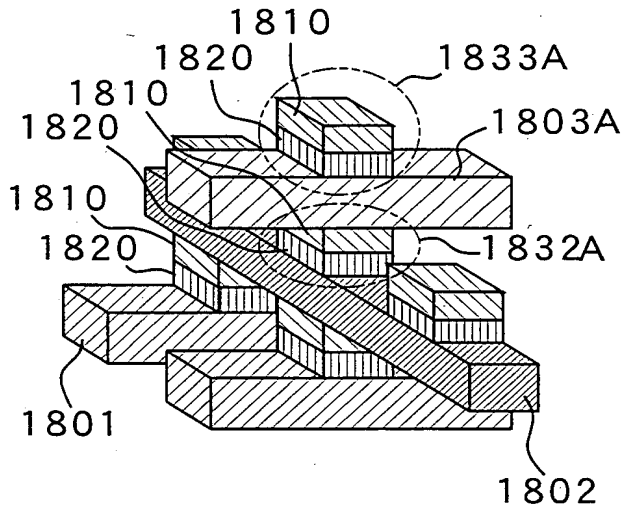


Fig. 18C

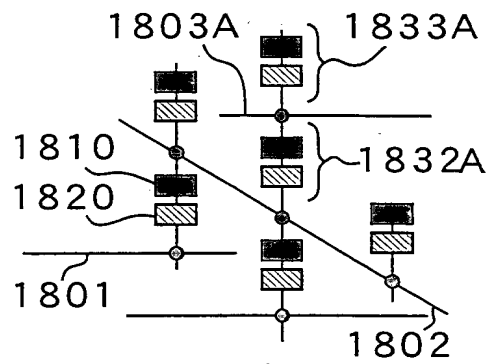


Fig. 18B

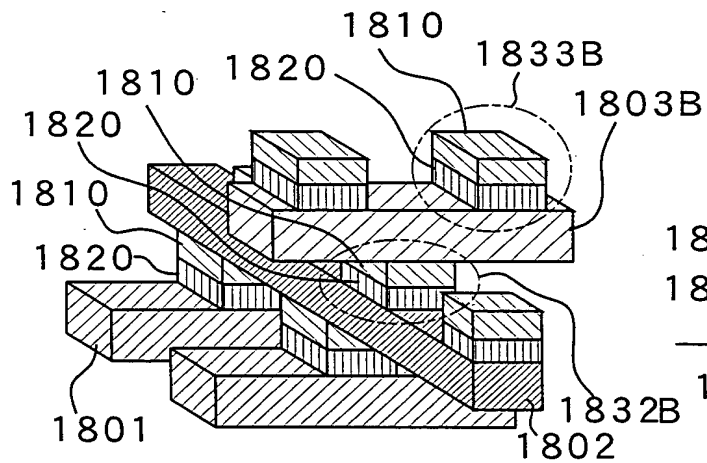
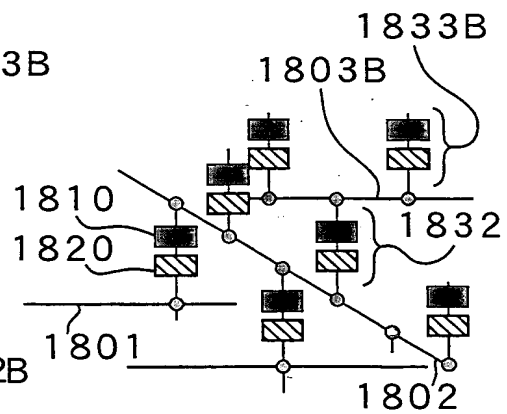
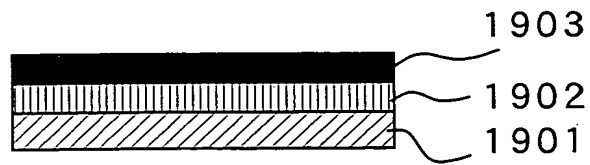
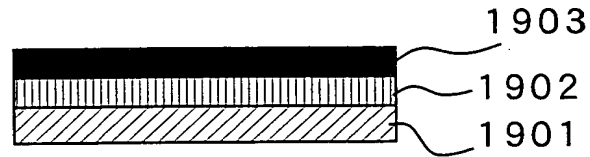
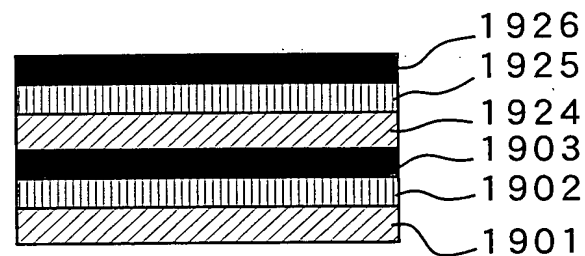
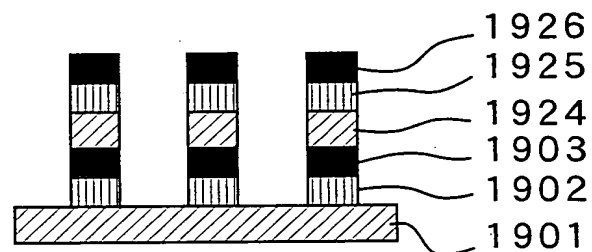
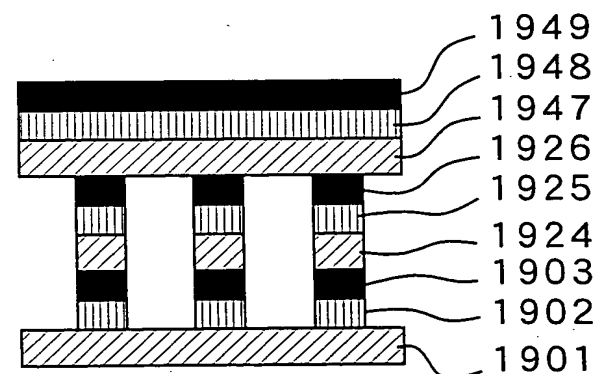


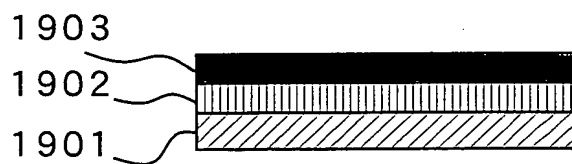
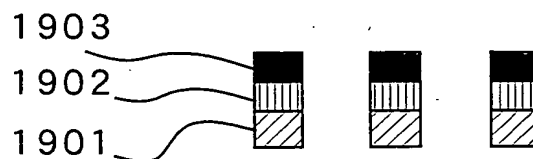
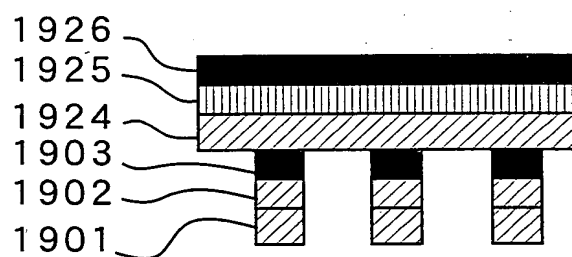
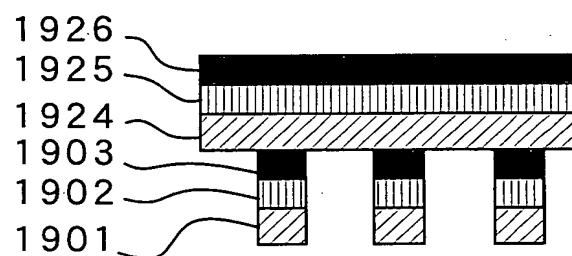
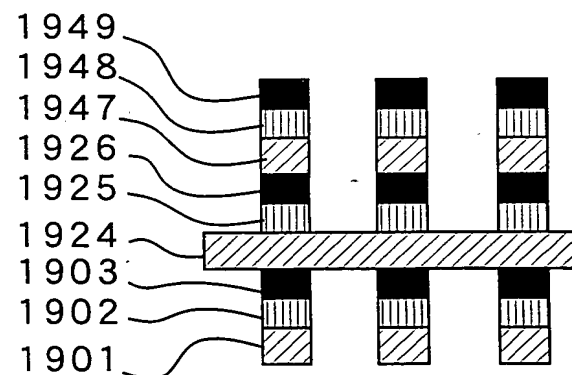
Fig. 18D

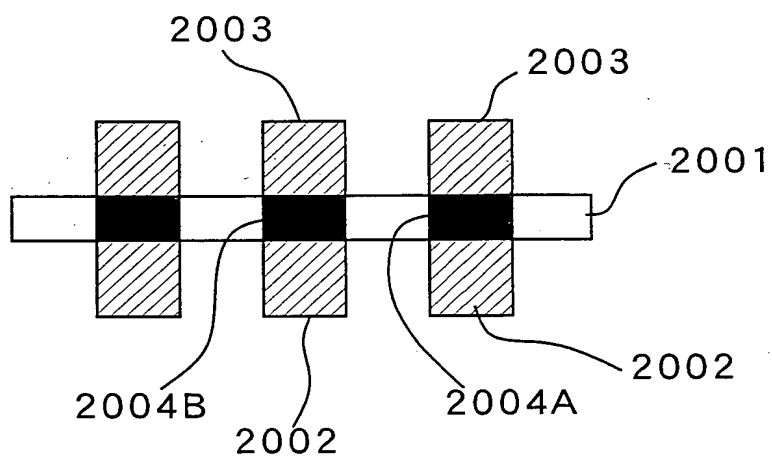
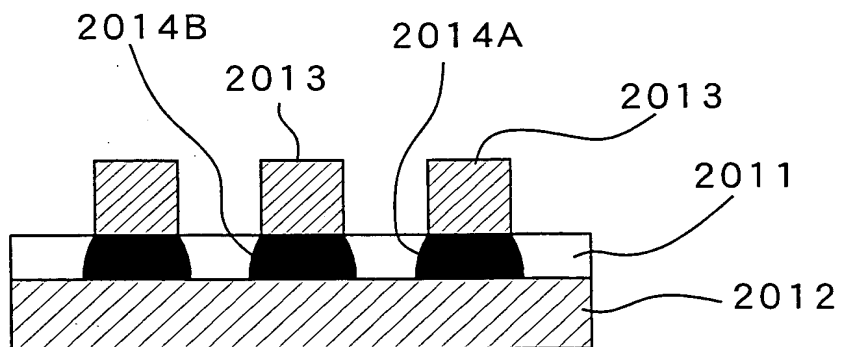


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*Fig. 19A**Fig. 19B**Fig. 19C**Fig. 19D**Fig. 19E*

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*Fig. 19F**Fig. 19G**Fig. 19H**Fig. 19I**Fig. 19J*

*Fig.20A**Fig.20B*

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Fig. 21A

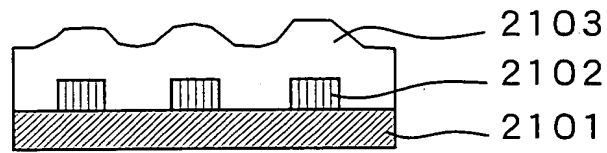


Fig. 21B

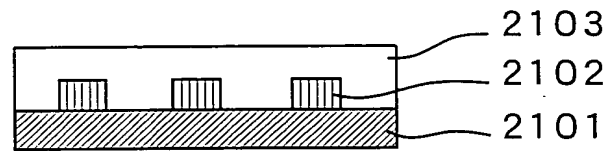


Fig. 21C

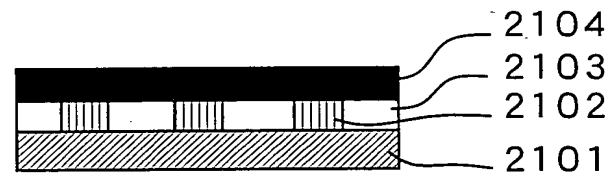


Fig. 21D

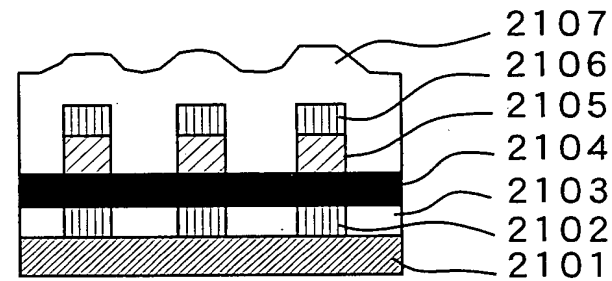
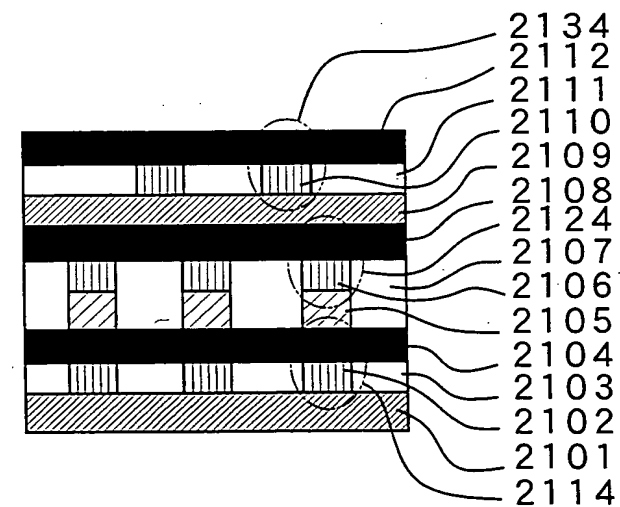
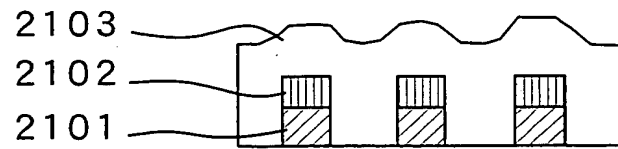
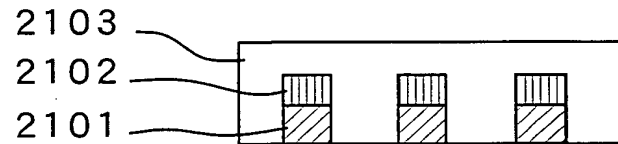
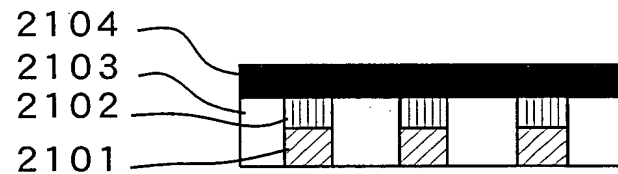
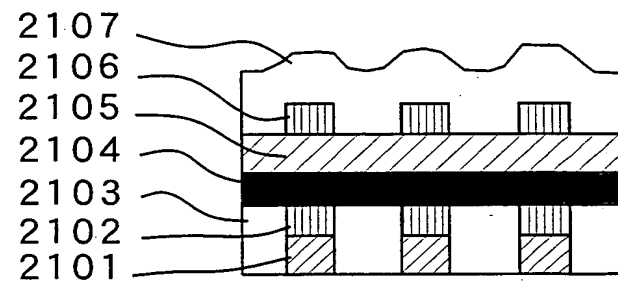
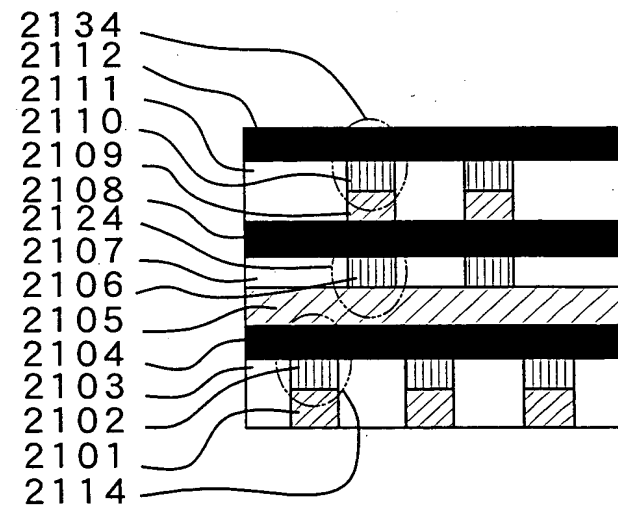


Fig. 21E



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*Fig.21F**Fig.21G**Fig.21H**Fig.21I**Fig.21J*

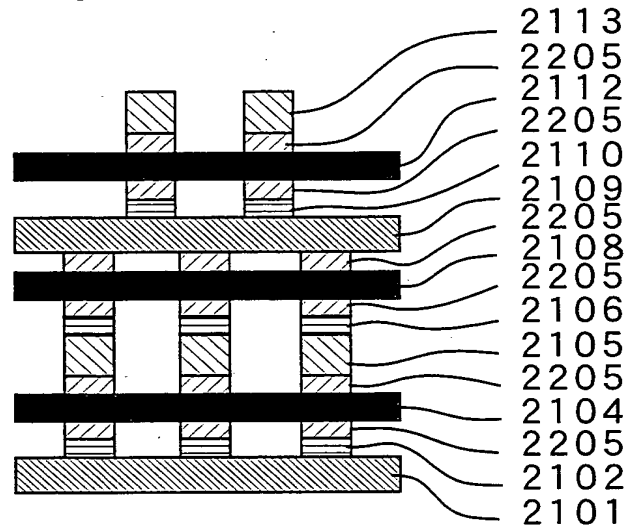
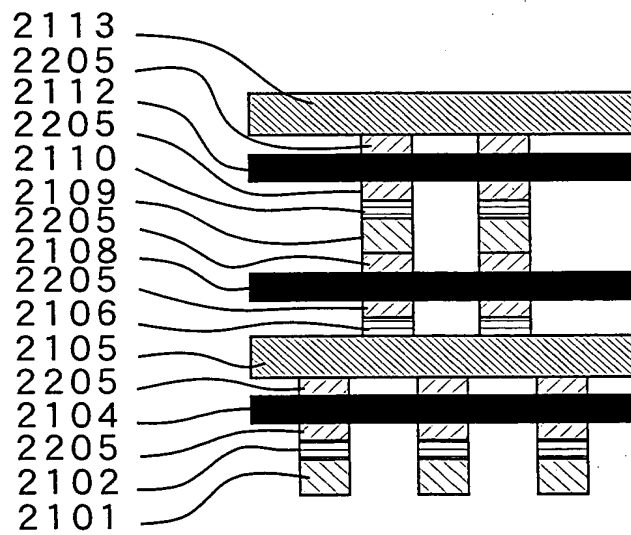
*Fig.22A**Fig.22B*

Fig. 23A

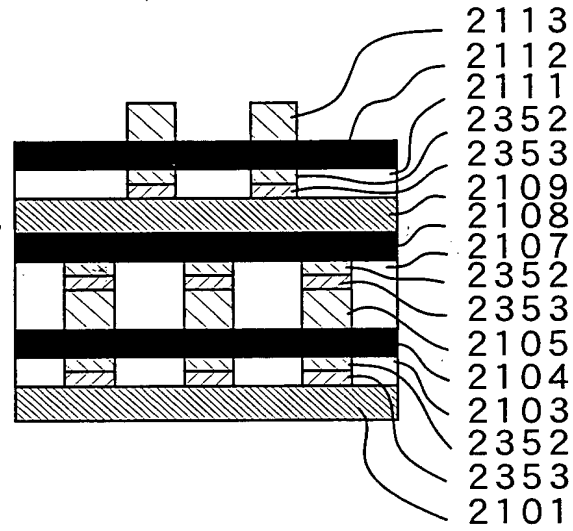


Fig. 23B

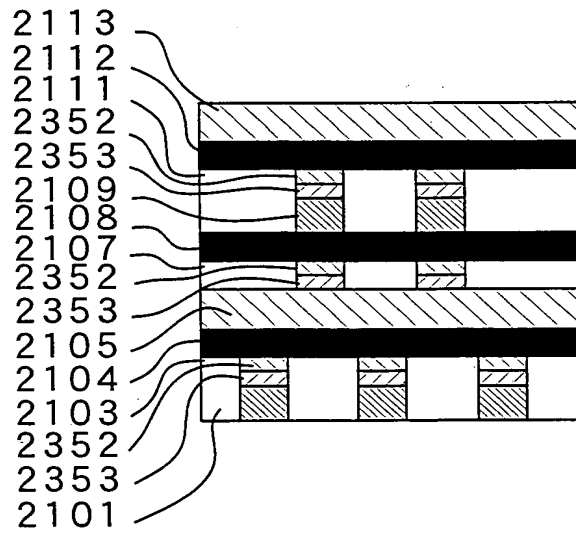


Fig. 24A

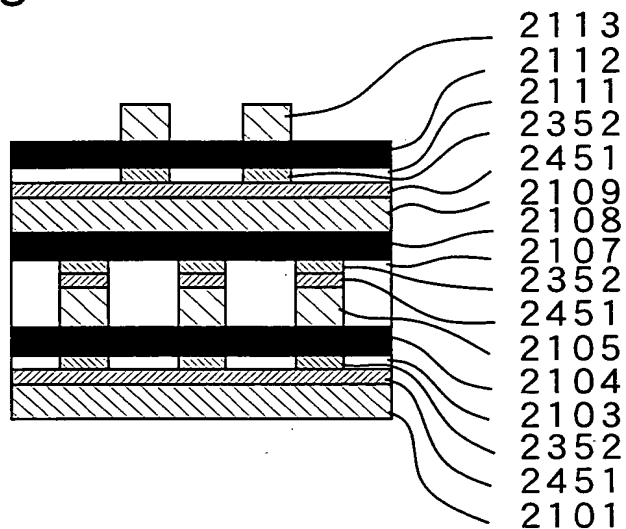
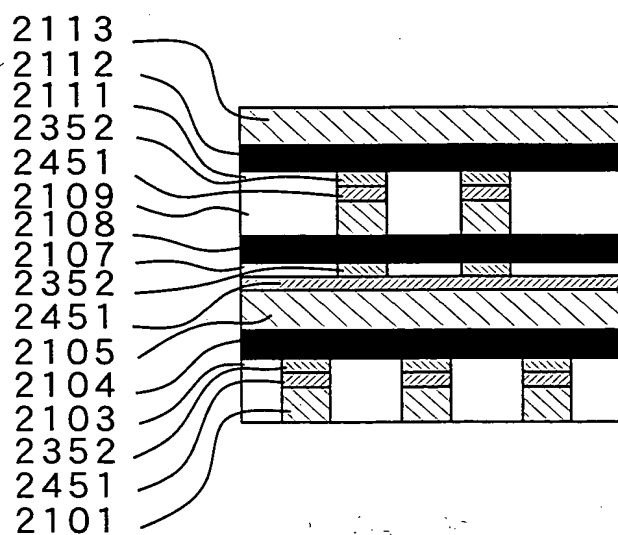
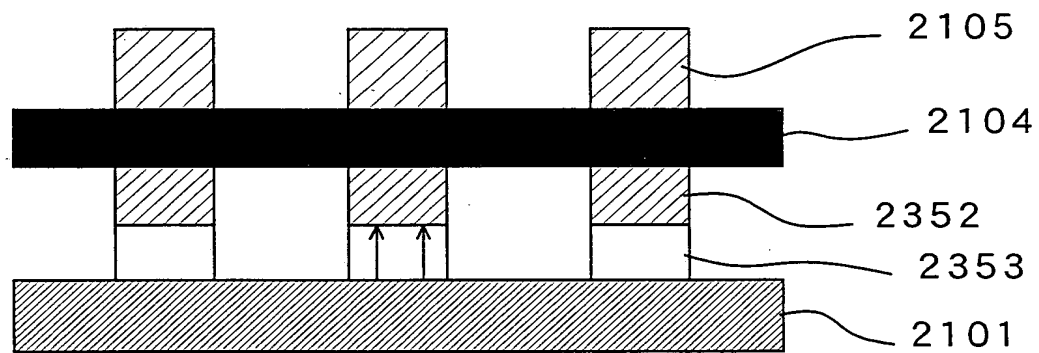
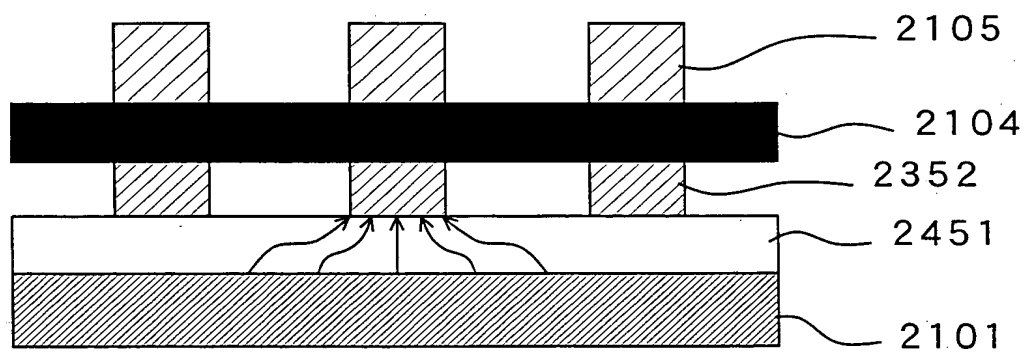
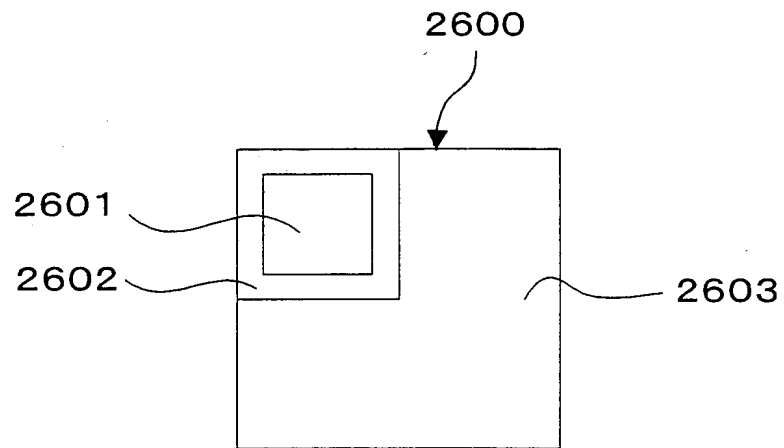
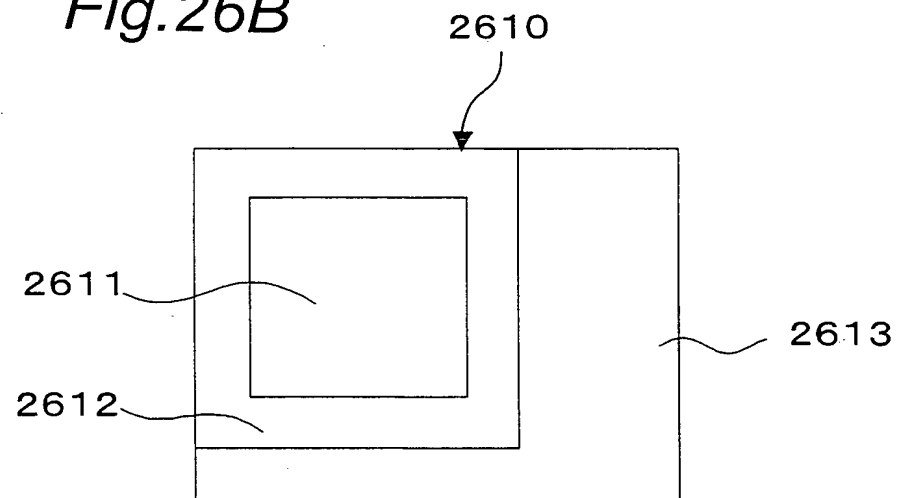
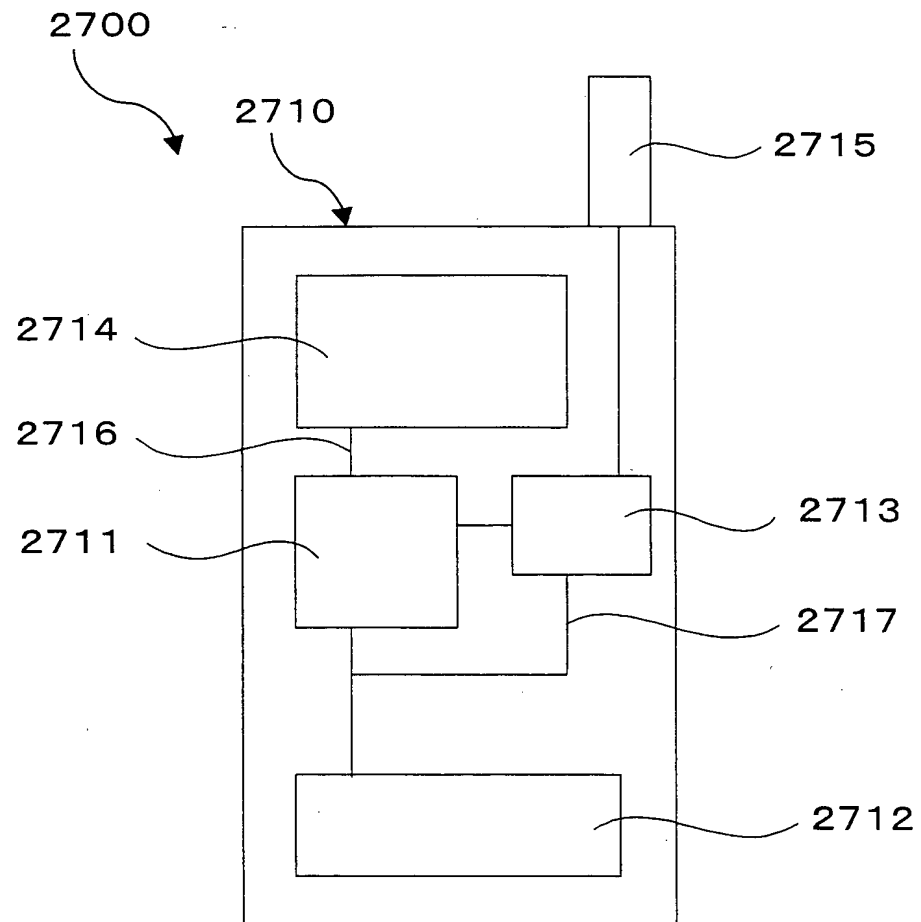


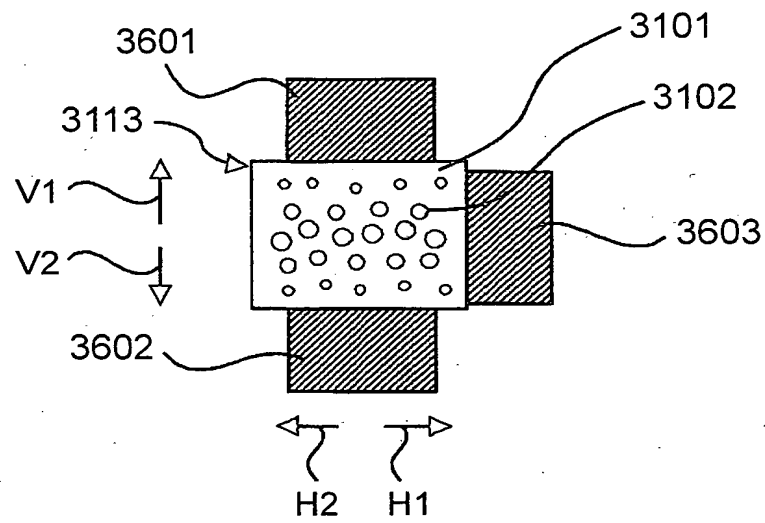
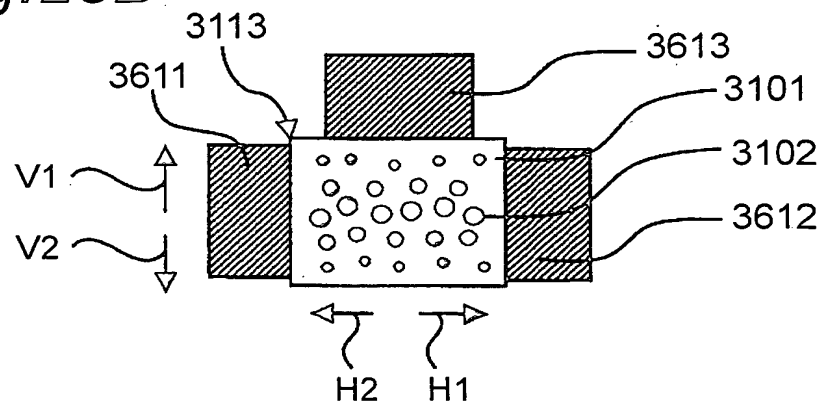
Fig. 24B



*Fig.25A**Fig.25B*

*Fig. 26A**Fig. 26B*

*Fig.27*

*Fig. 28A**Fig. 28B*

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Fig. 29A

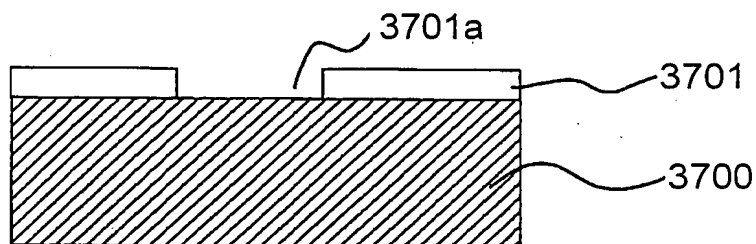


Fig. 29B

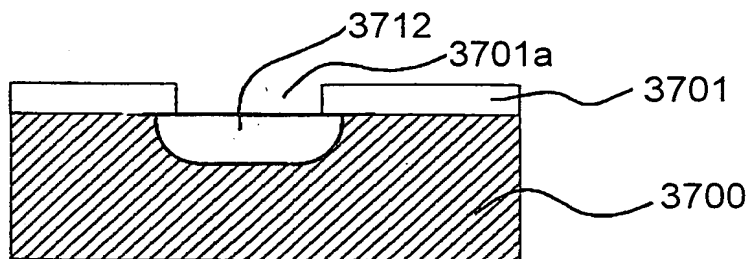


Fig. 29C

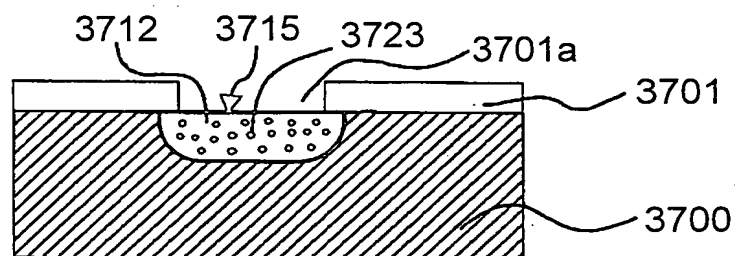


Fig. 29D

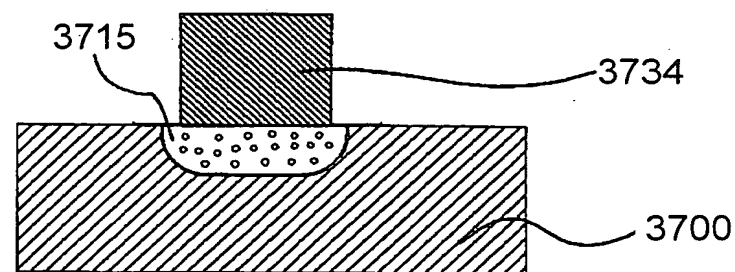


Fig. 29E

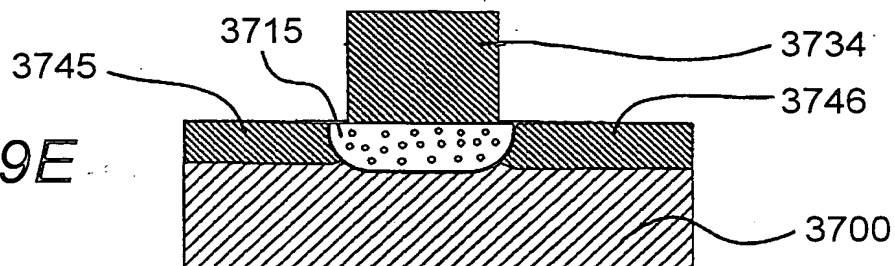


Fig. 30A

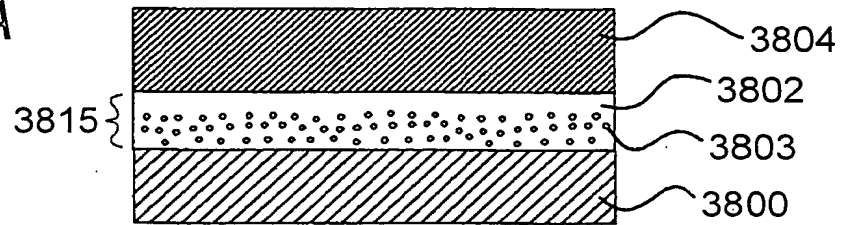


Fig. 30B

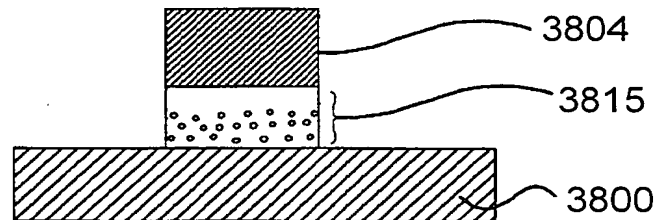


Fig. 30C

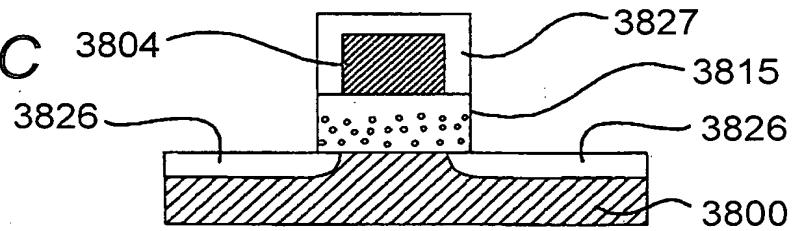


Fig. 30D

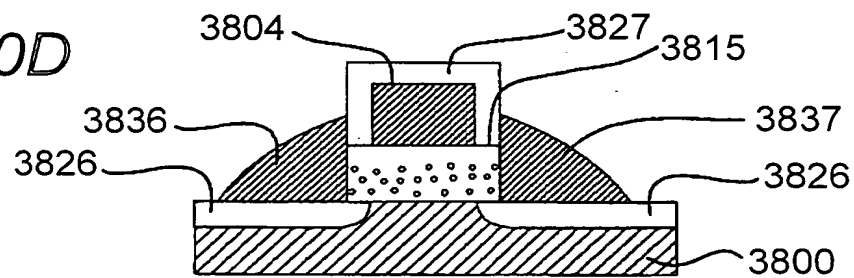


Fig. 30E

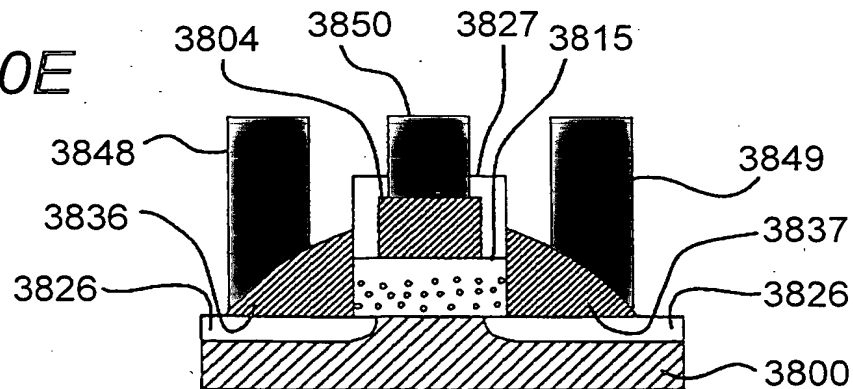


Fig.31A

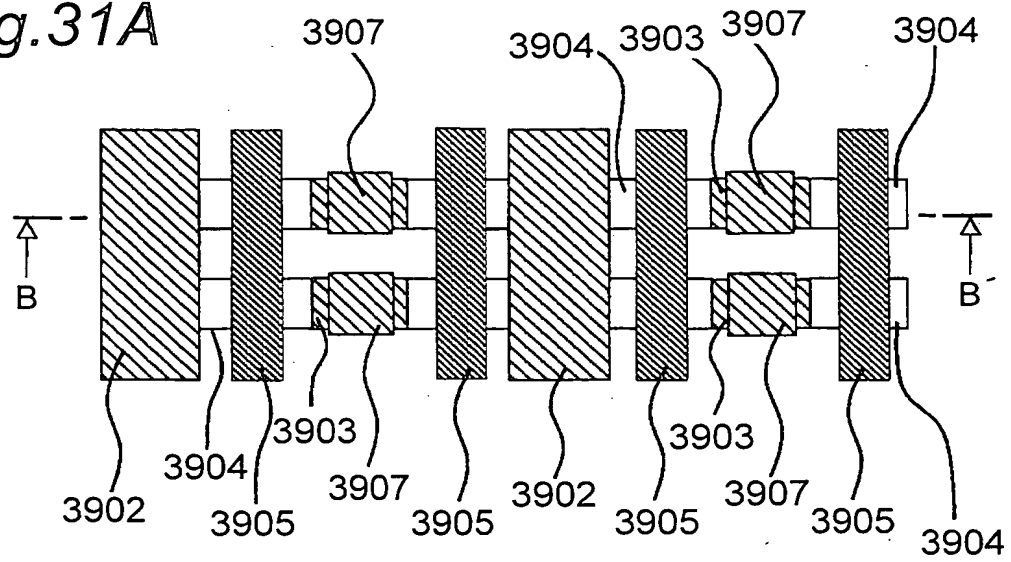
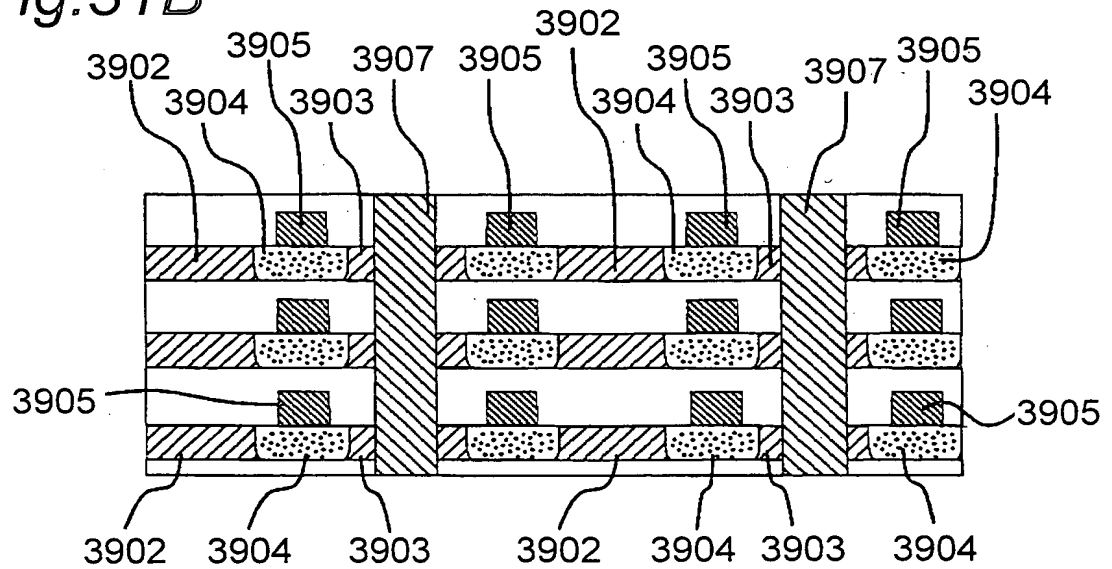
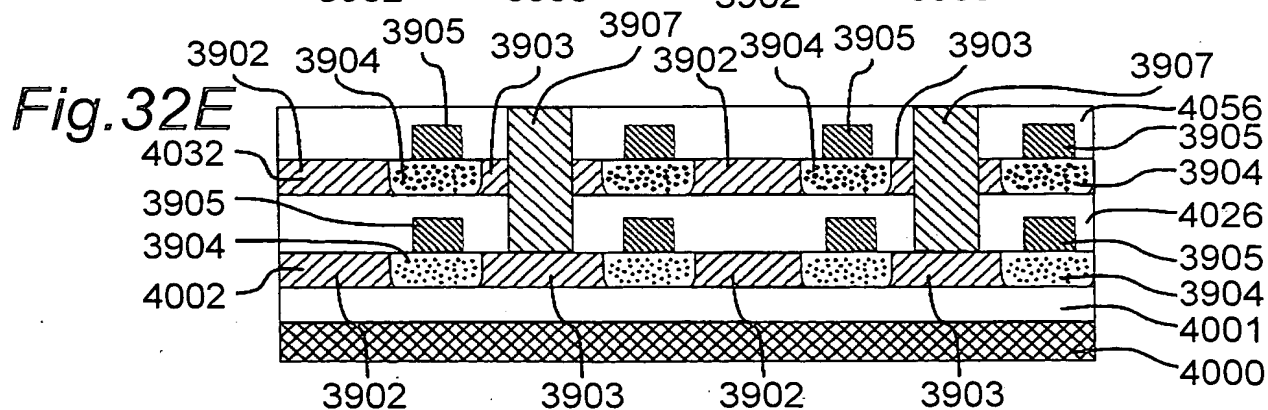
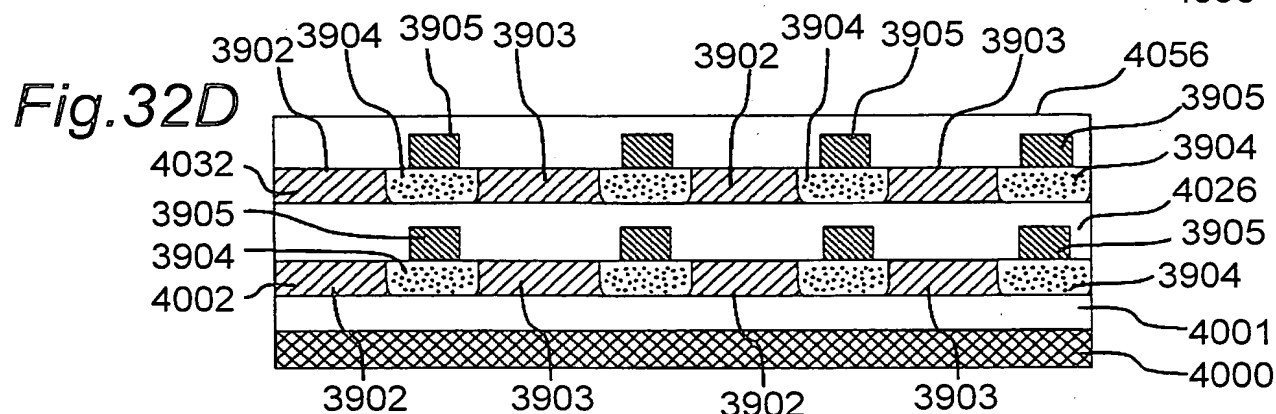
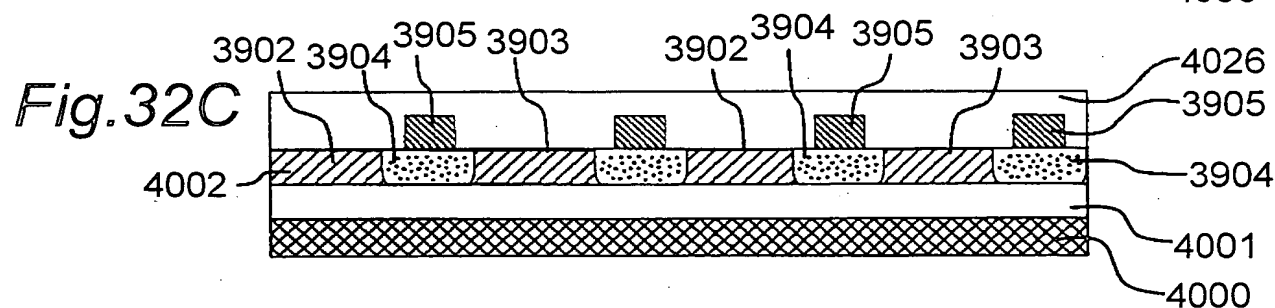
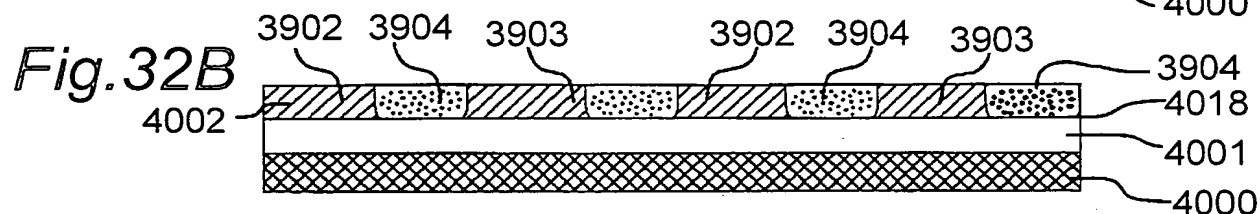
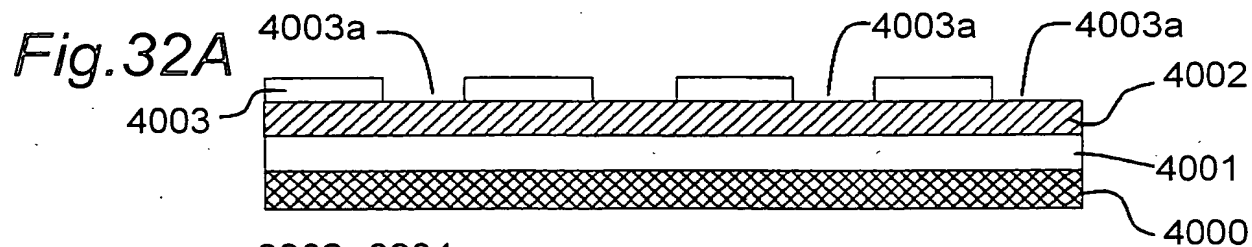


Fig.31B





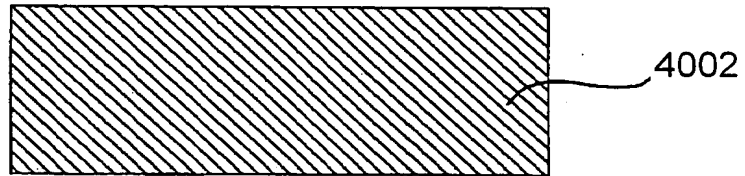
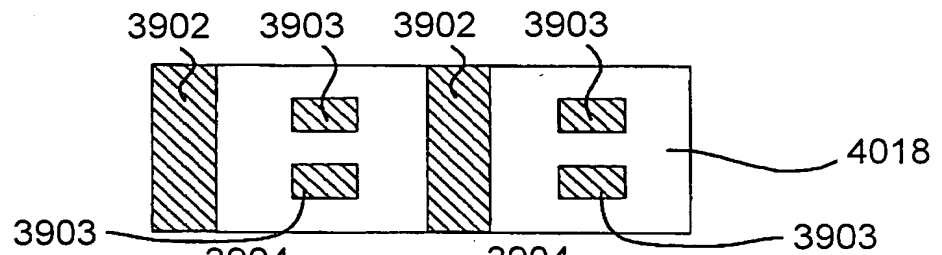
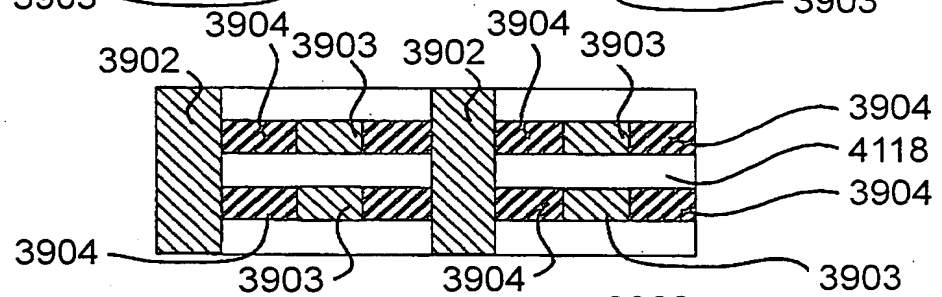
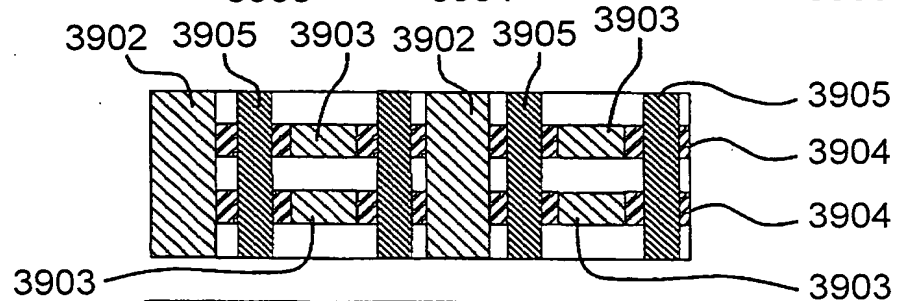
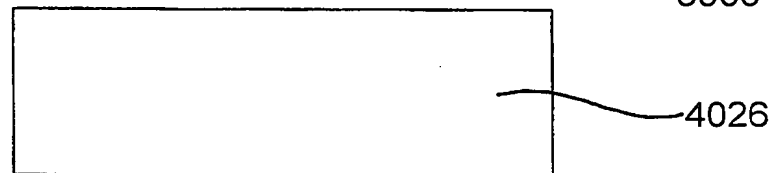
*Fig. 33A**Fig. 33B**Fig. 33C**Fig. 33D**Fig. 33E**Fig. 33F*

Fig.34A

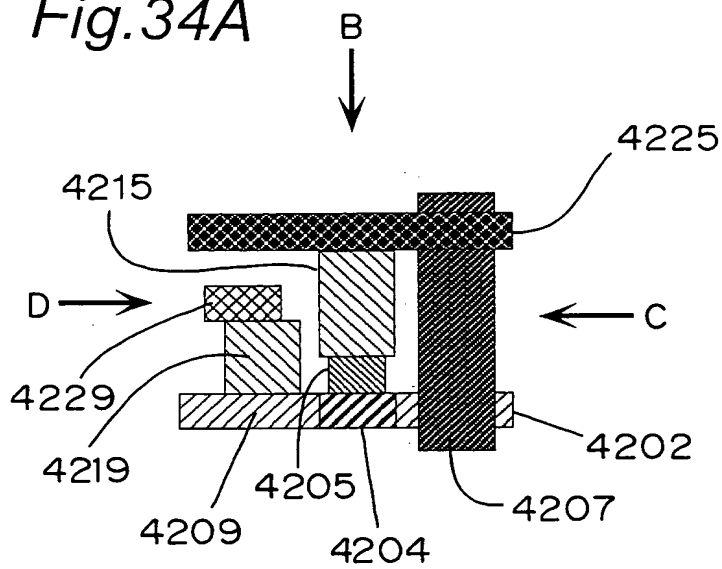


Fig.34B

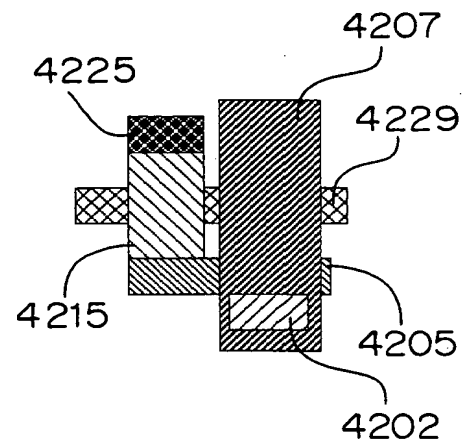


Fig.34C

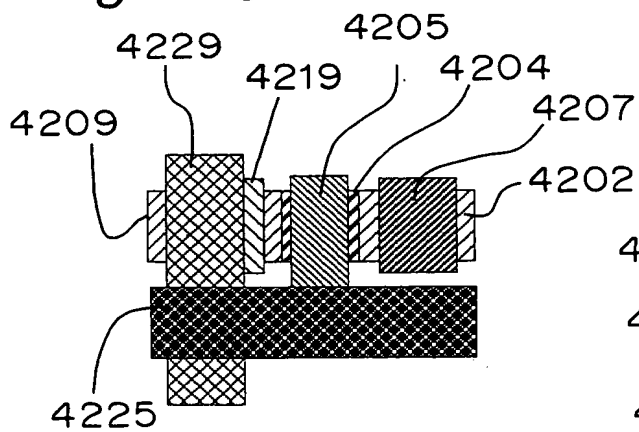
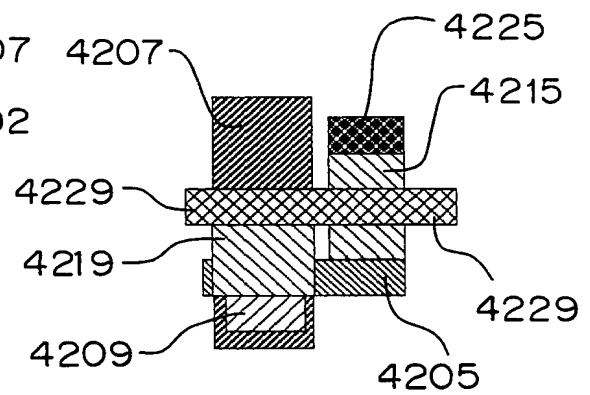


Fig.34D



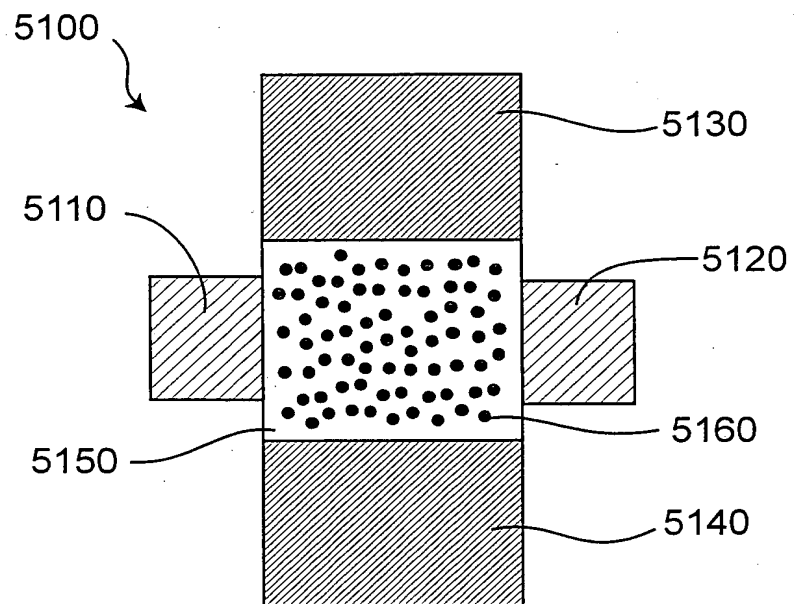
*Fig.35*

Fig. 36

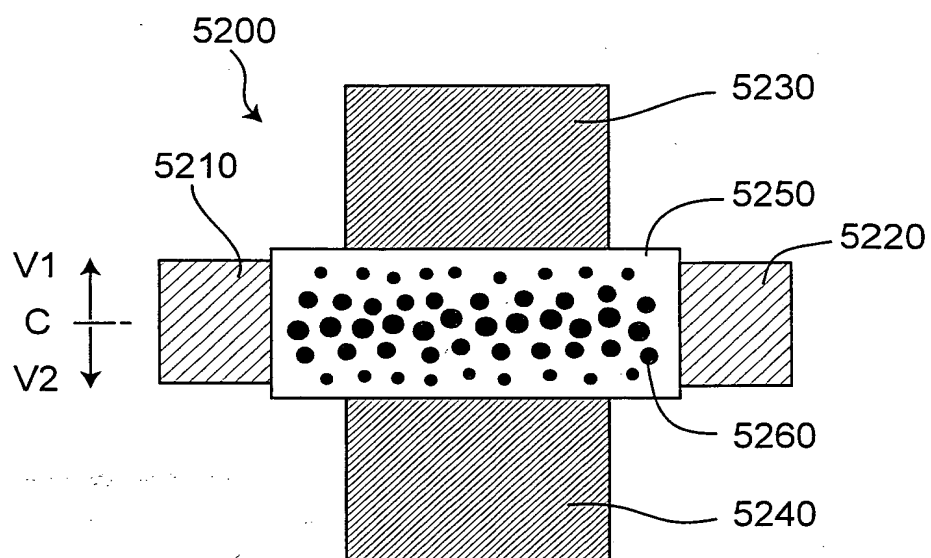


Fig.37A

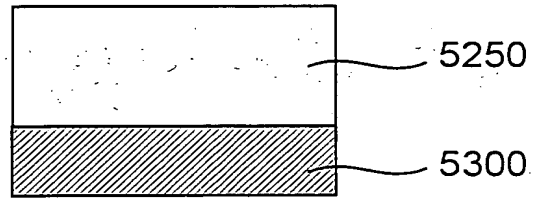


Fig.37B

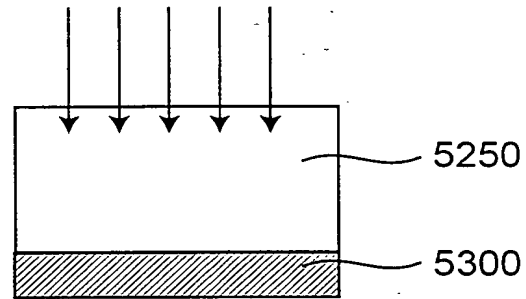


Fig.37C

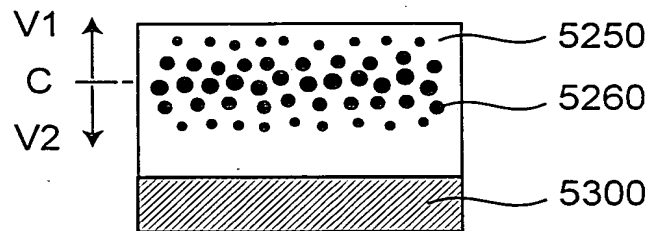


Fig.37D

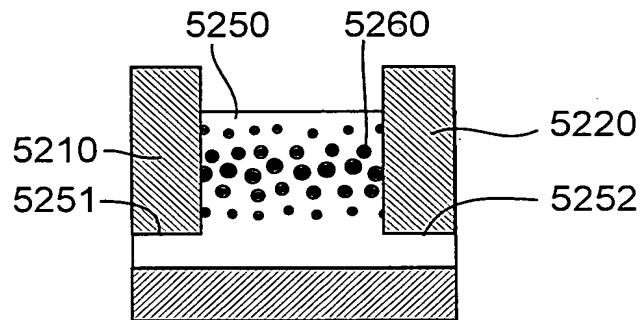
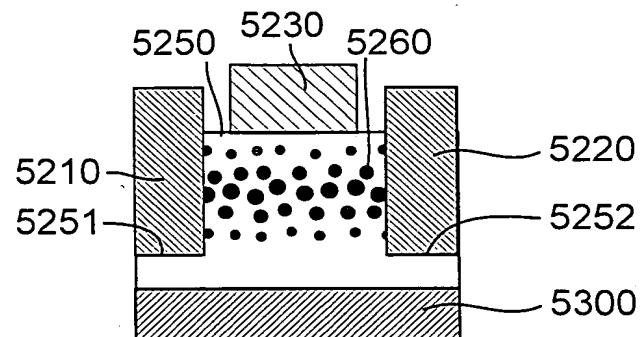
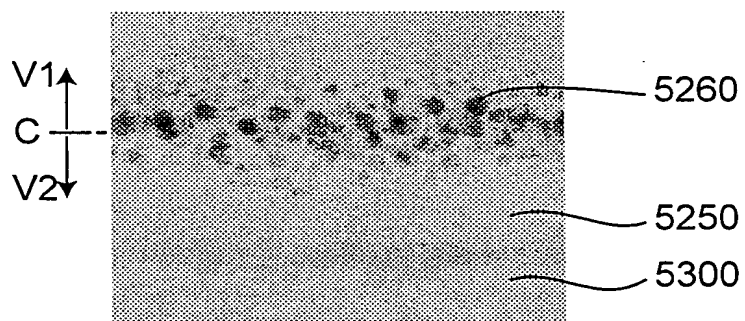
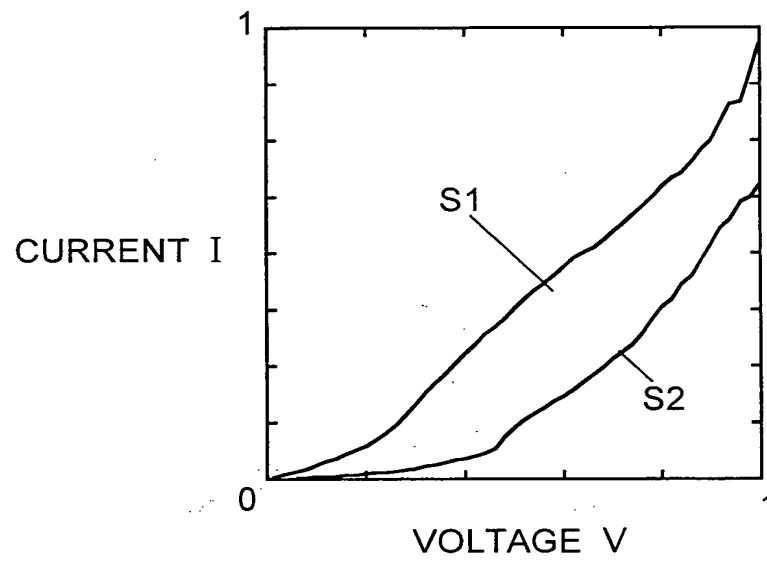


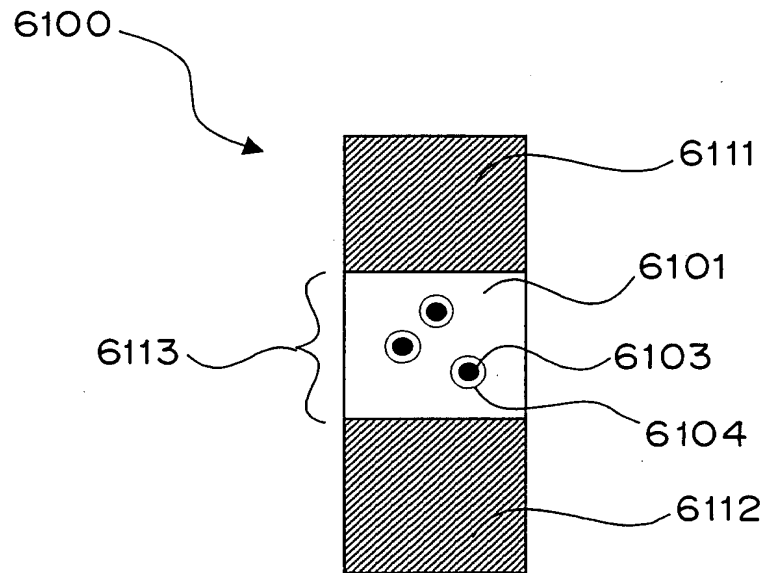
Fig.37E



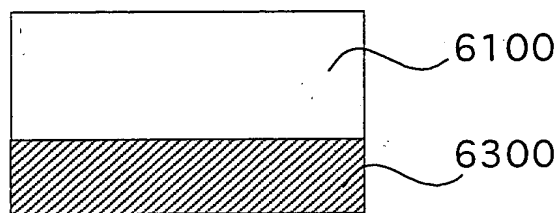
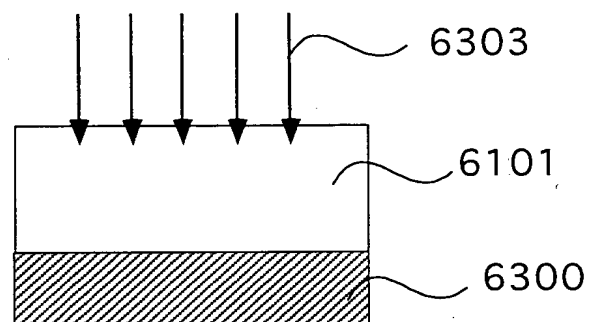
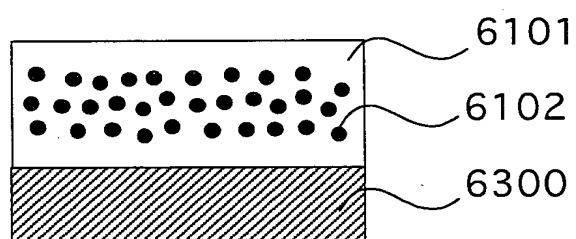
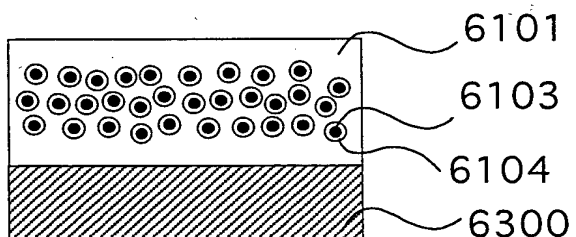
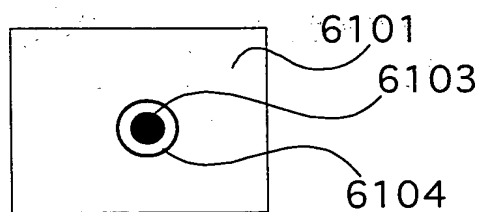
*Fig.38*

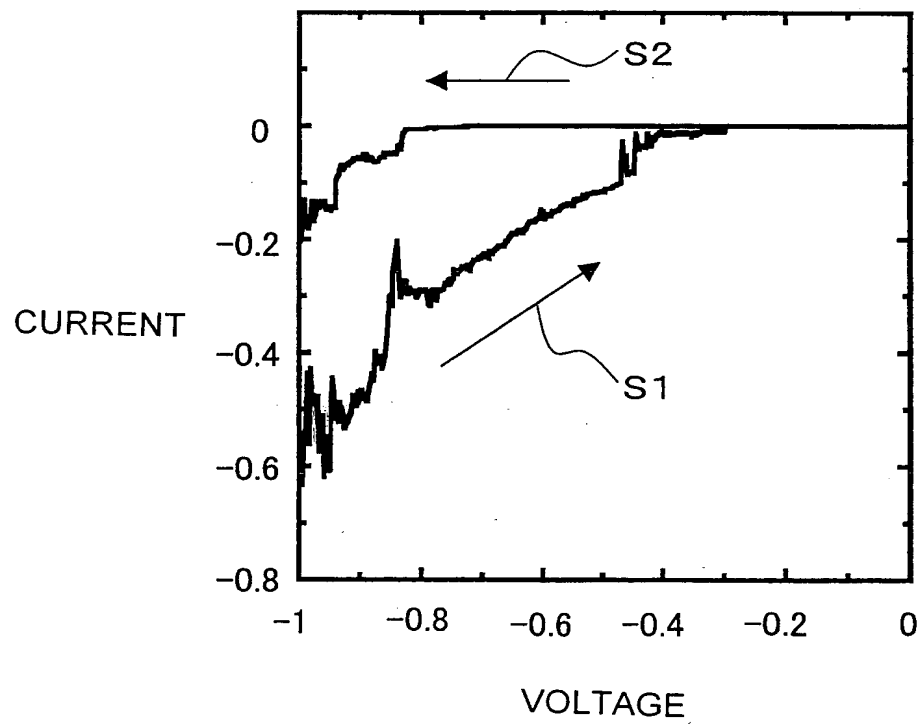


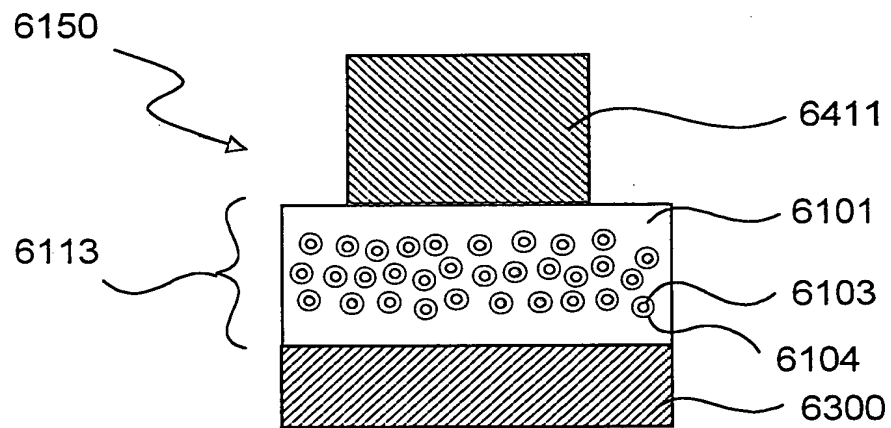
*Fig.39*

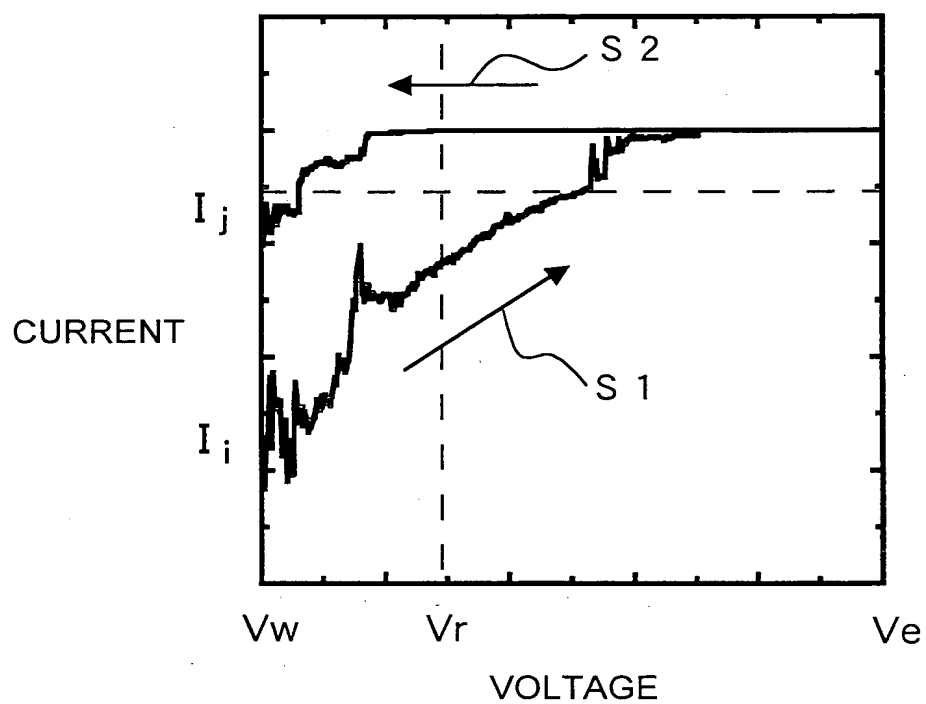
*Fig.40*

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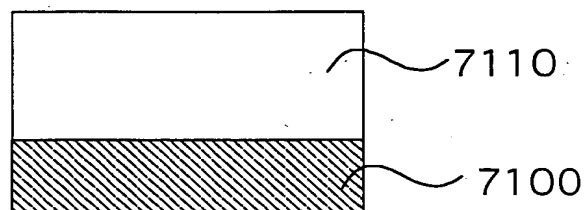
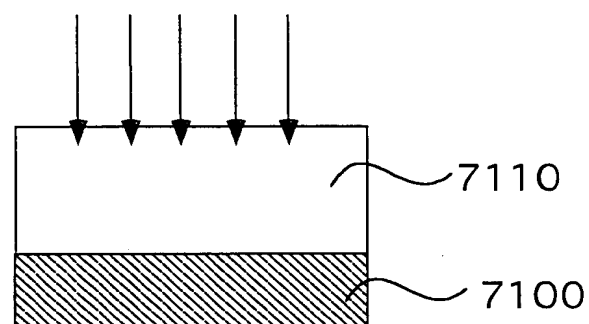
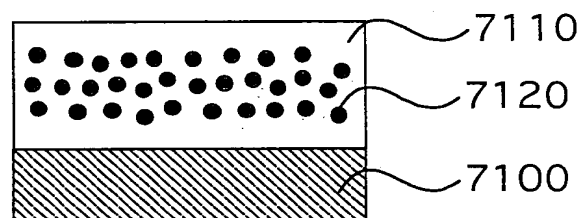
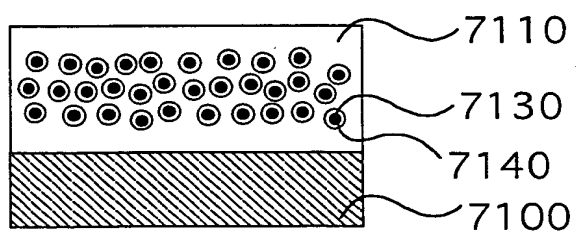
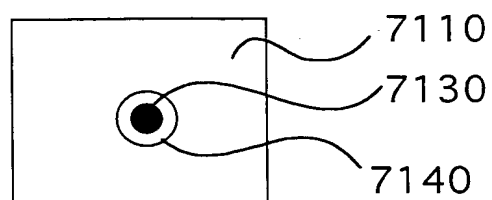
*Fig. 41A**Fig. 41B**Fig. 41C**Fig. 41D**Fig. 41E*

*Fig.42*

*Fig. 43*

*Fig.44*

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*Fig.45A**Fig.45B**Fig.45C**Fig.45D**Fig.45E*

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Fig.46A

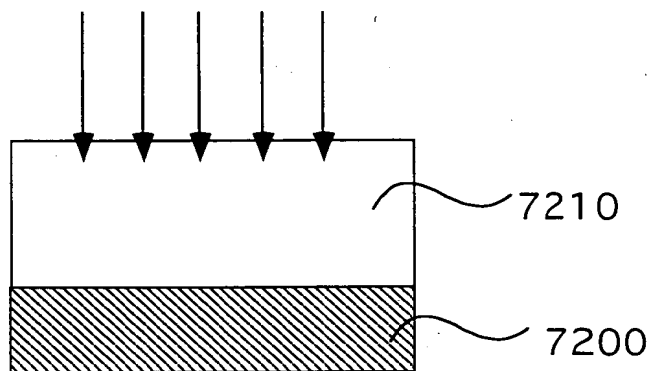


Fig.46B

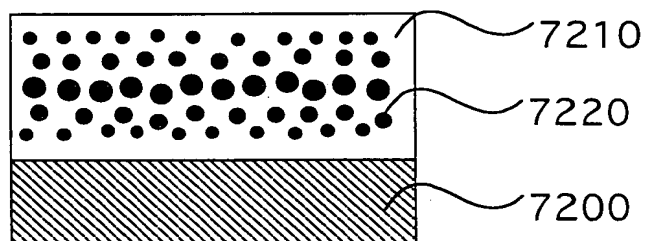


Fig.46C

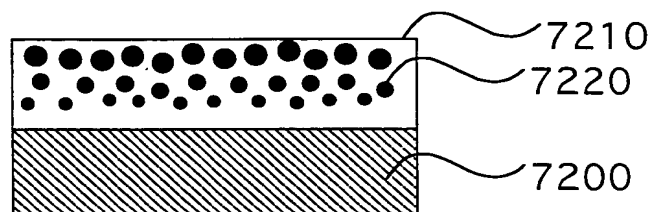
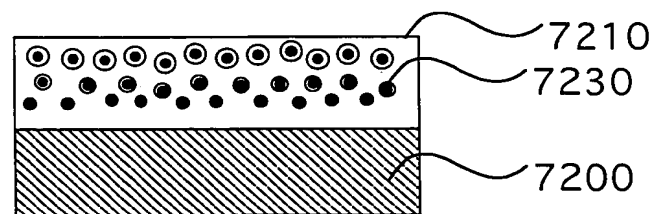


Fig.46D



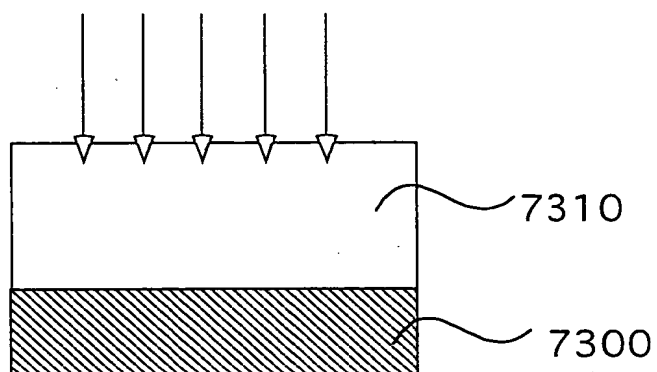
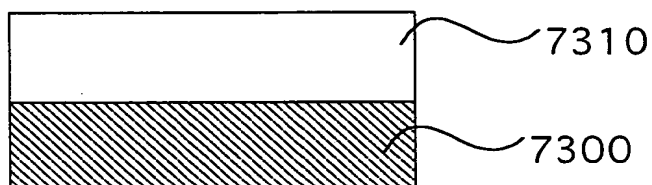
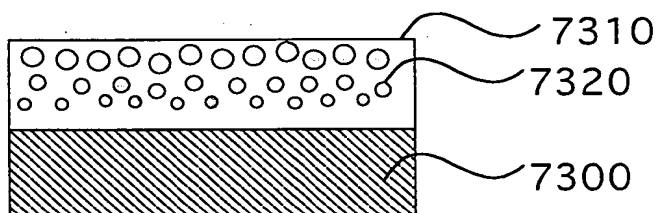
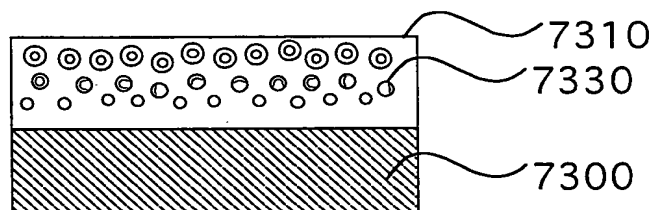
*Fig.47A**Fig.47B**Fig.47C**Fig.47D*

Fig.48A

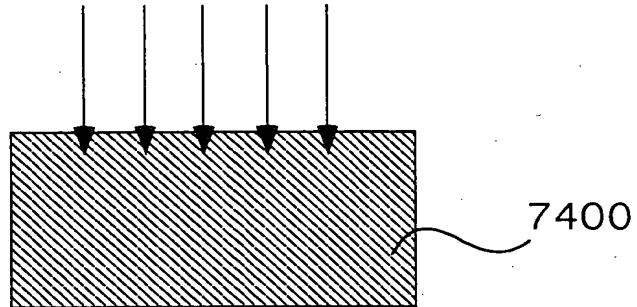


Fig.48B

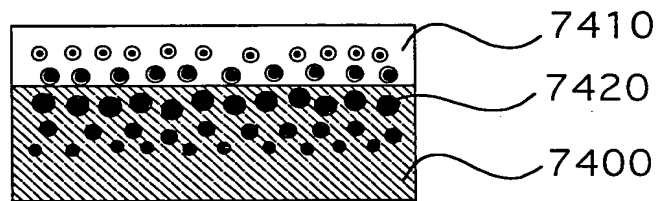


Fig.48C

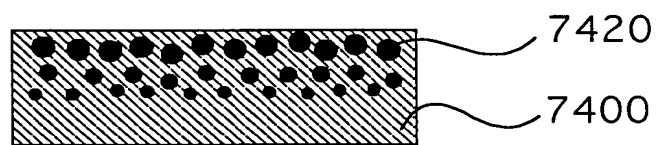
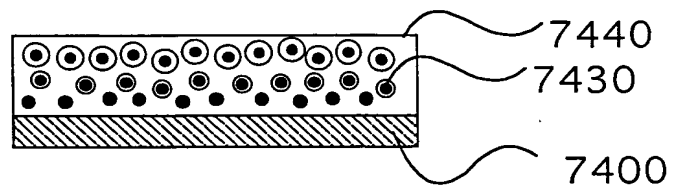
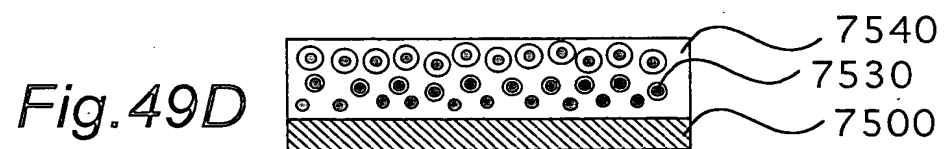
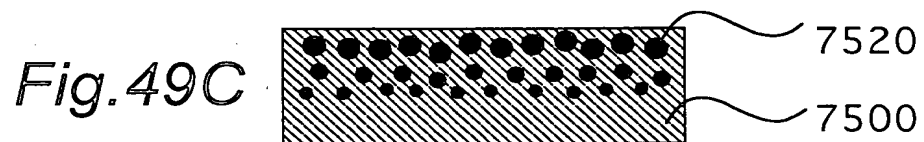
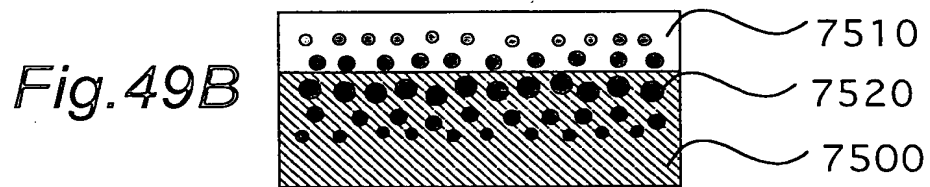
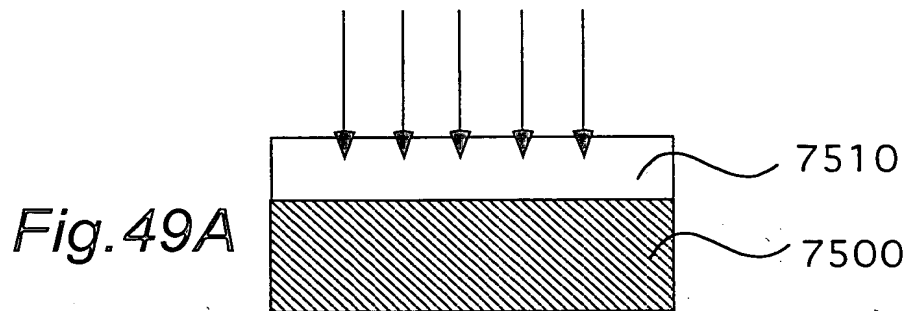
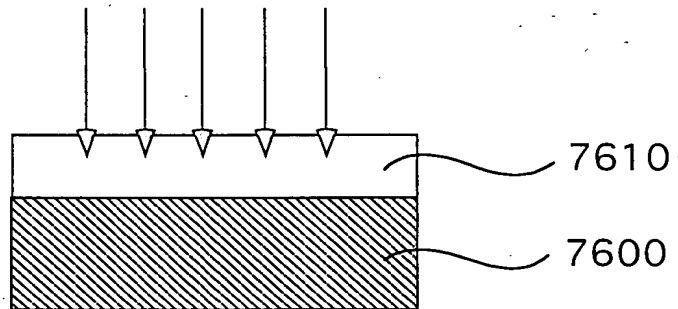
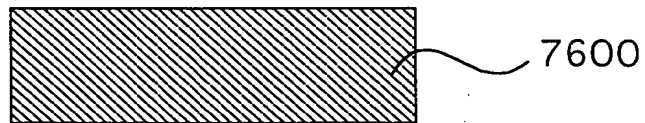
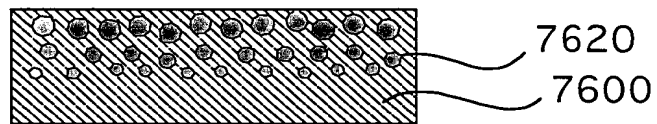
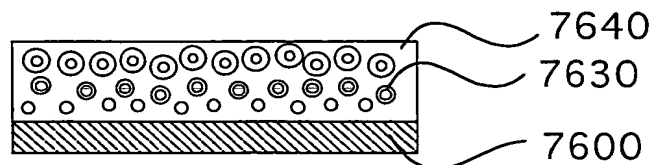


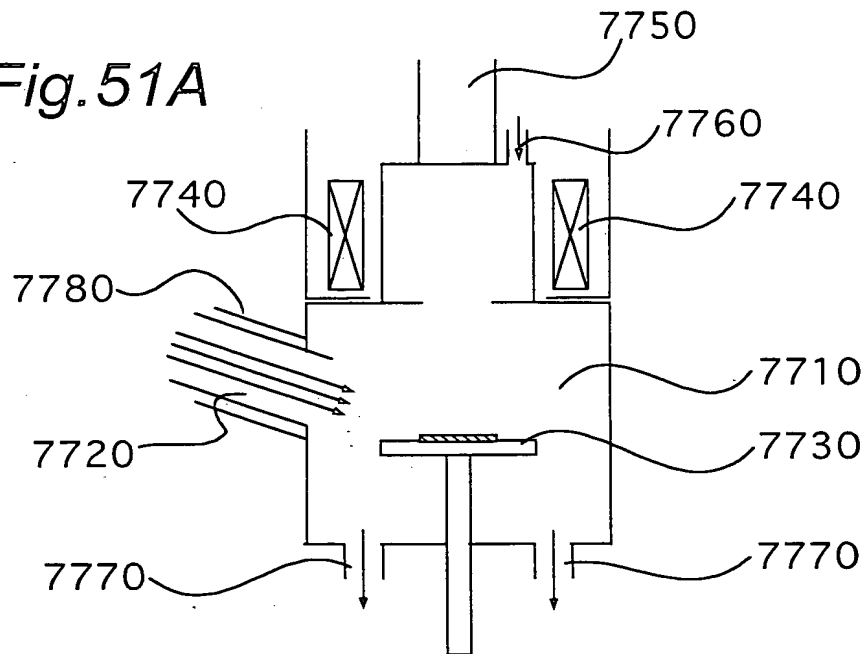
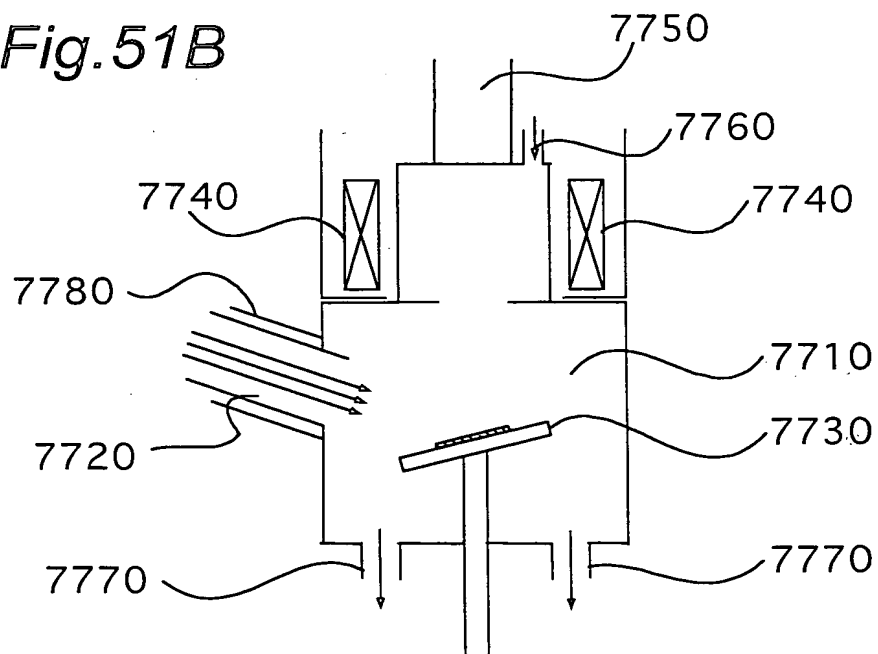
Fig.48D





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*Fig. 50A**Fig. 50B**Fig. 50C**Fig. 50D*

*Fig. 51A**Fig. 51B*

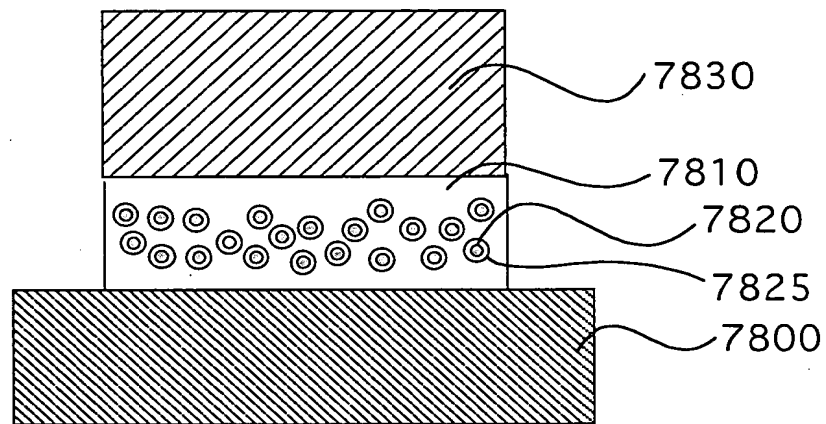
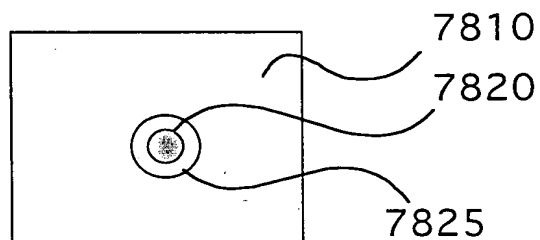
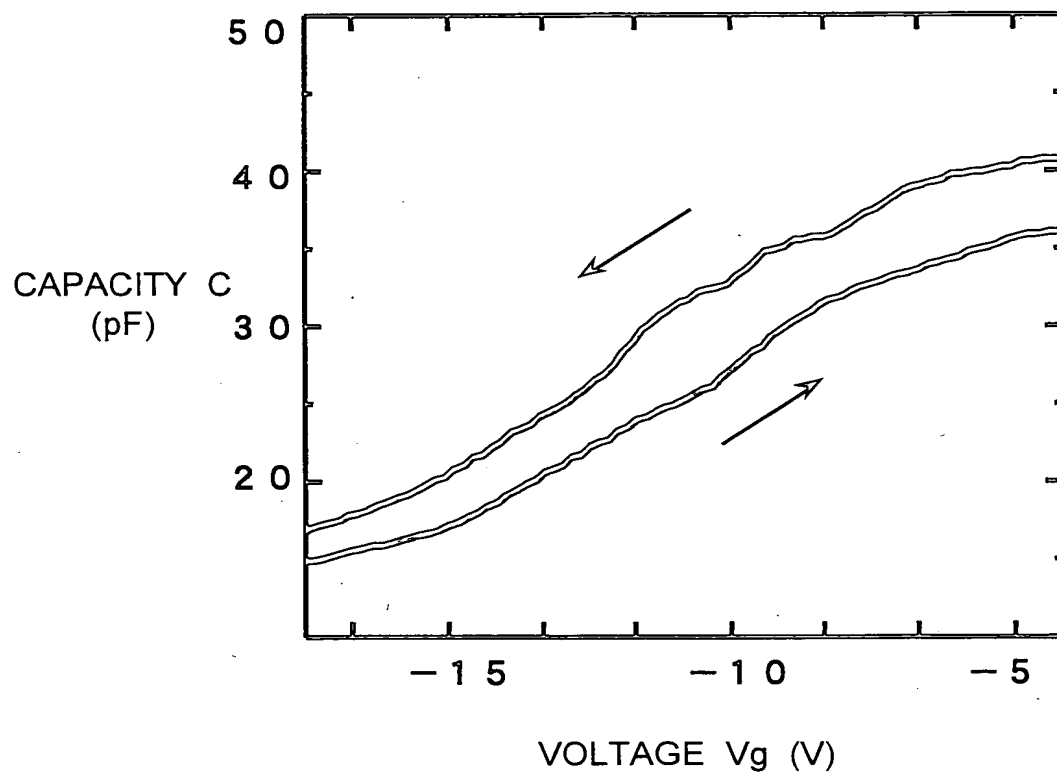
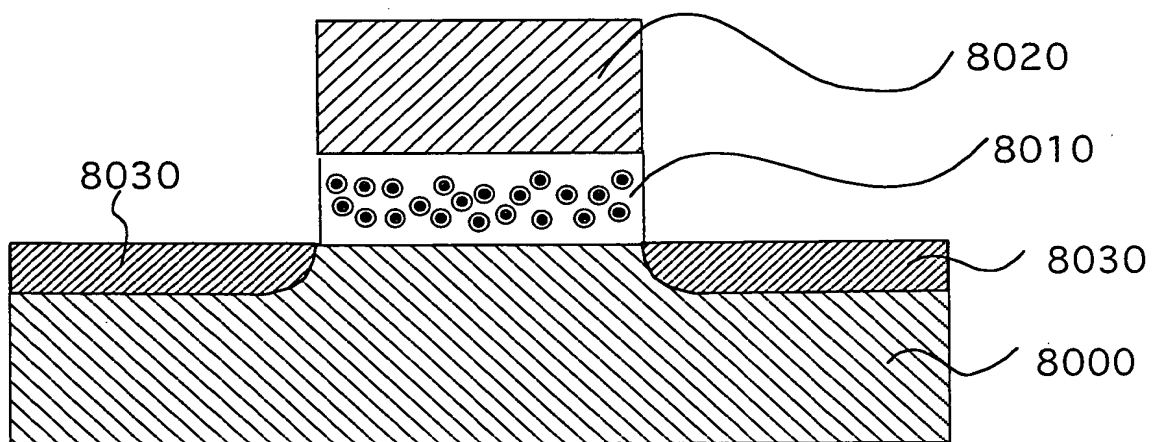
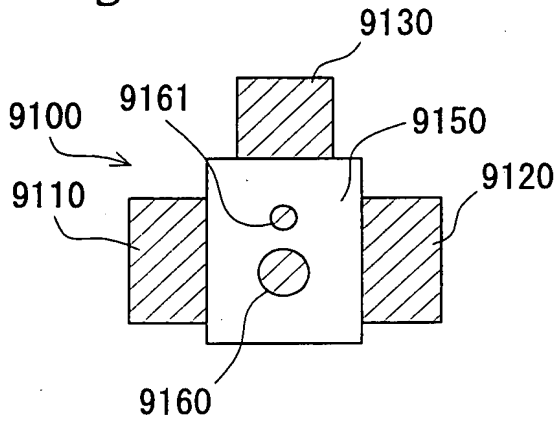
*Fig. 52A**Fig. 52B*

Fig. 53

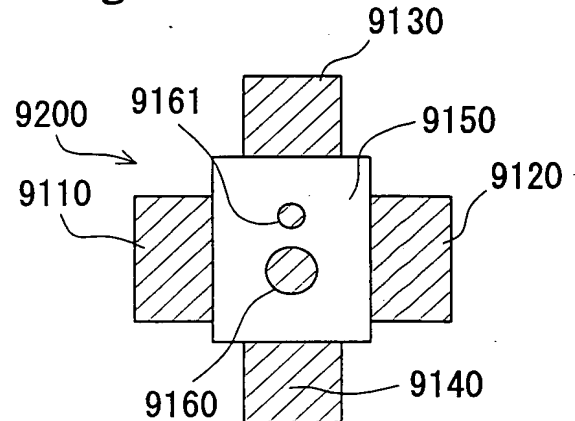


*Fig. 54*

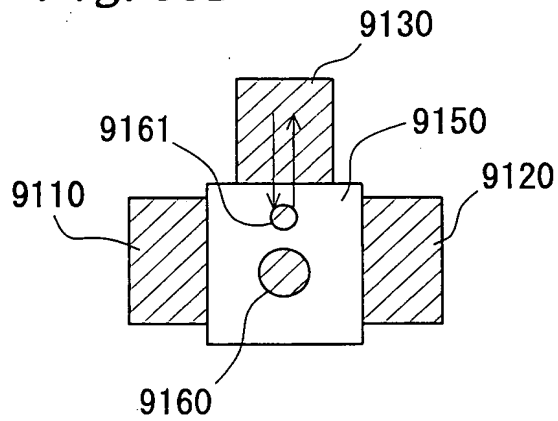
*Fig. 55A*



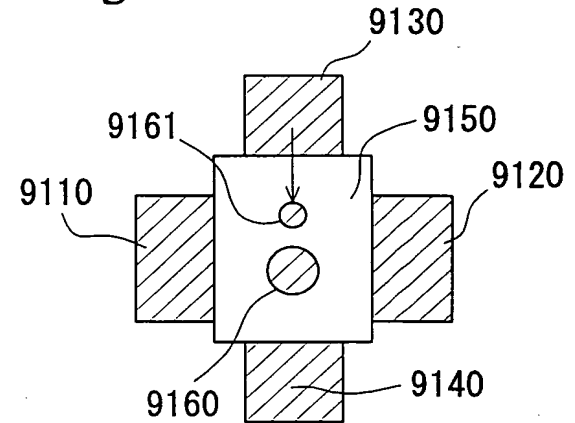
*Fig. 55D*



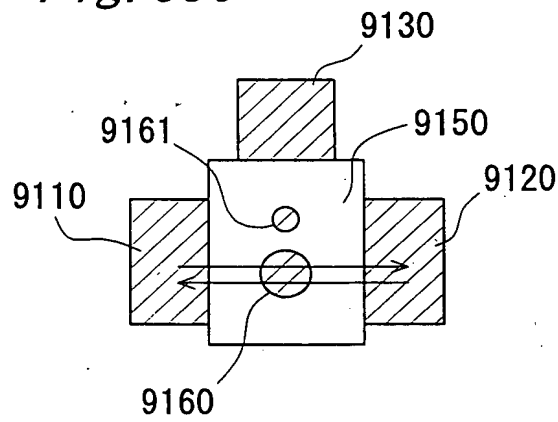
*Fig. 55B*



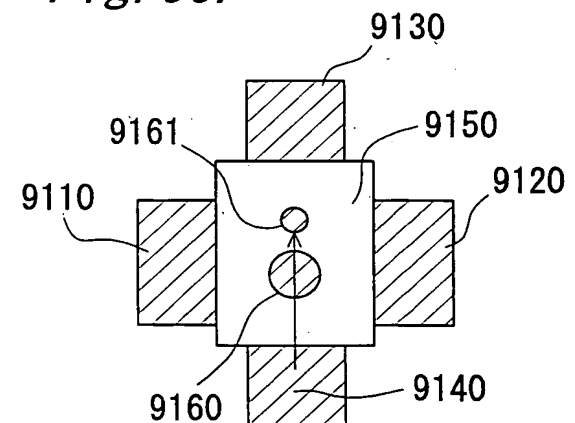
*Fig. 55E*



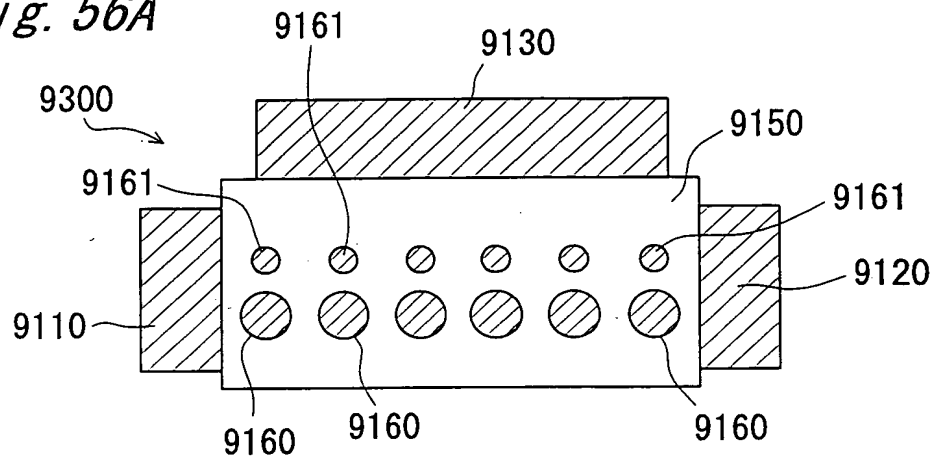
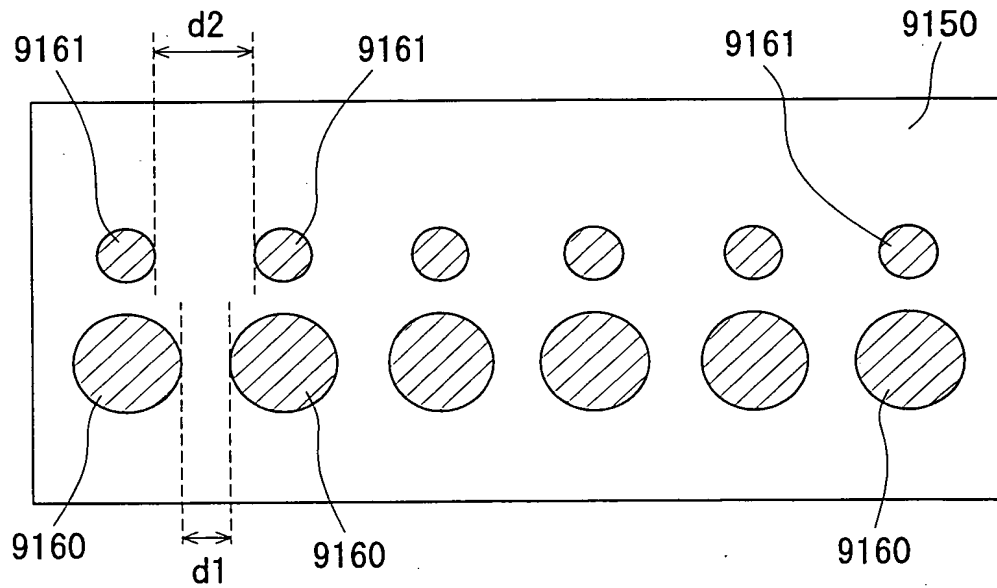
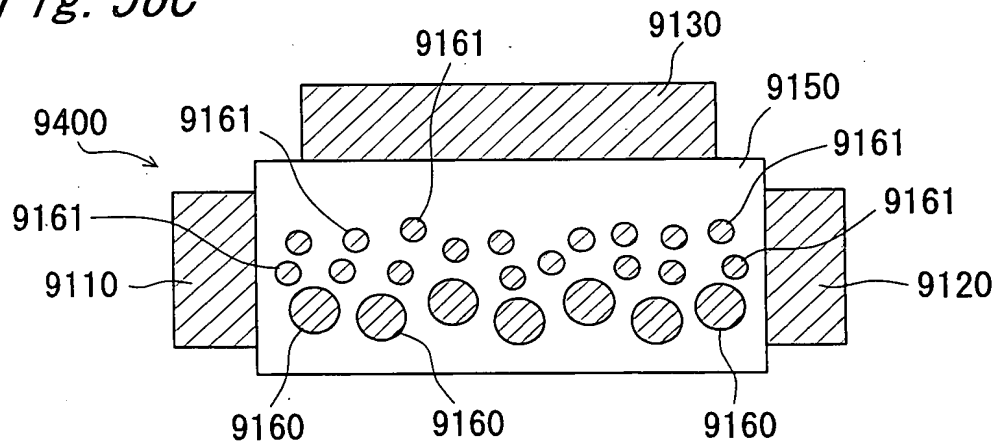
*Fig. 55C*

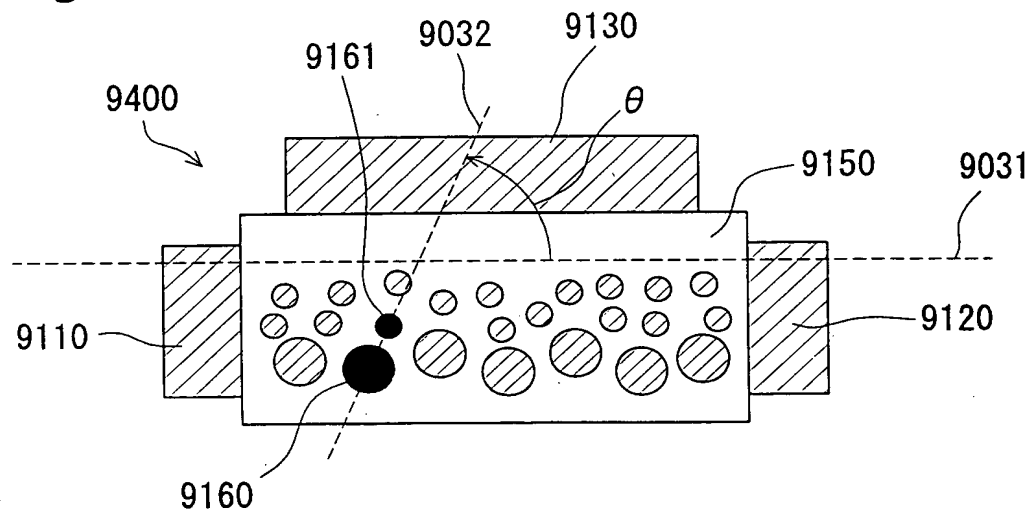


*Fig. 55F*



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*Fig. 56A**Fig. 56B**Fig. 56C*



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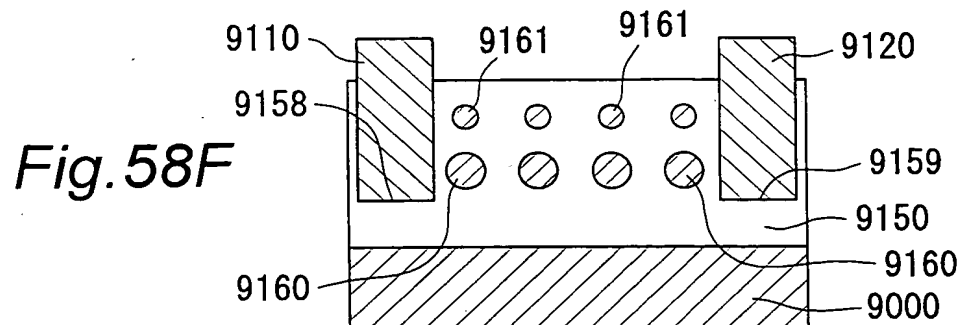
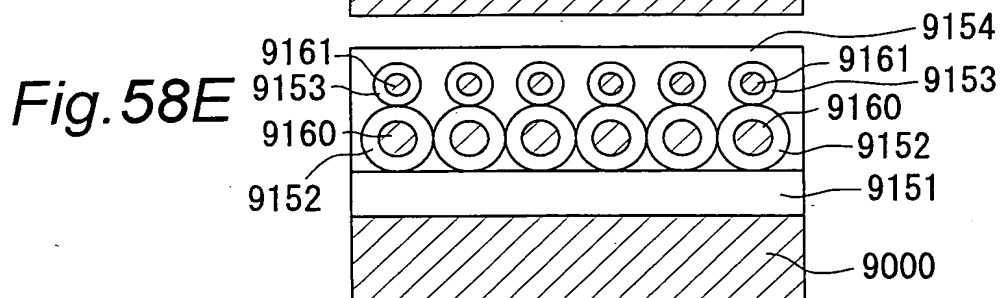
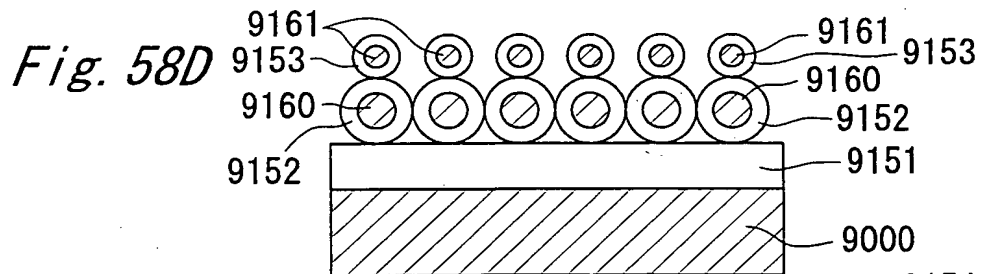
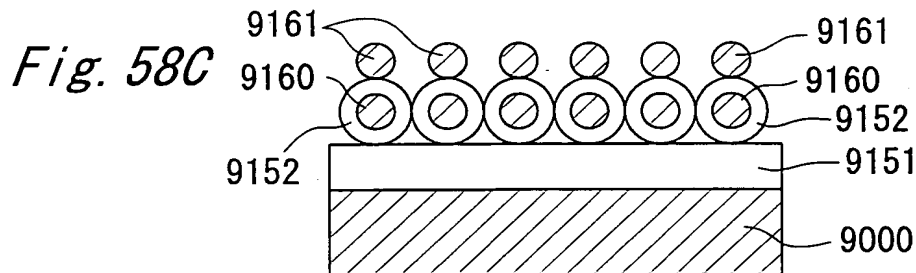
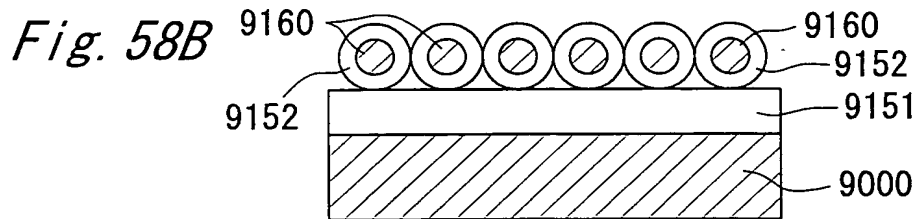
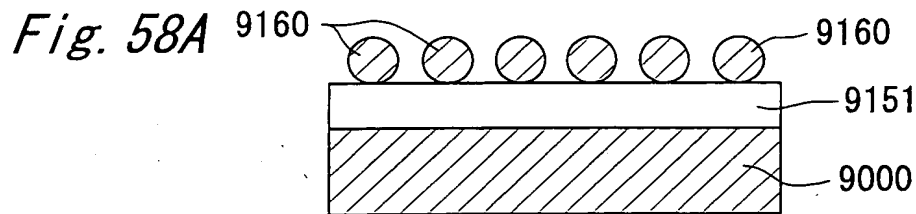


Fig. 59A

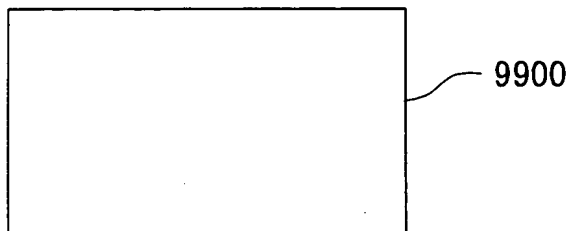


Fig. 59B

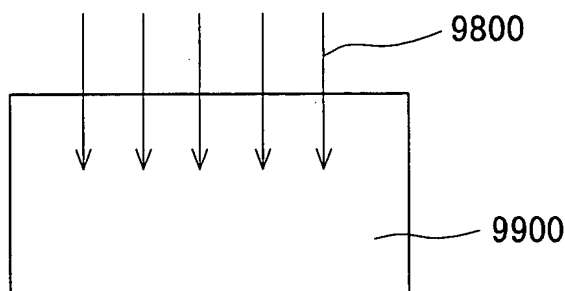


Fig. 59C

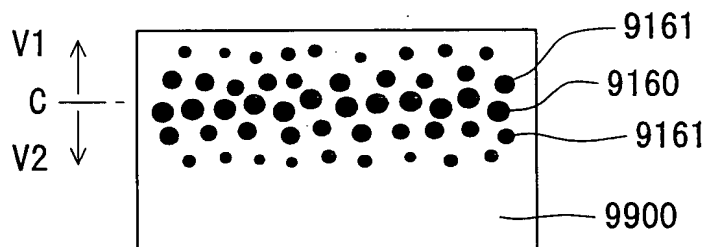


Fig. 59D

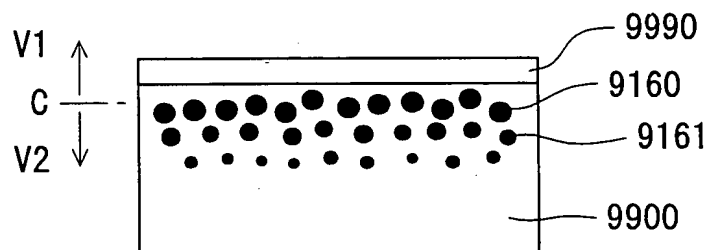
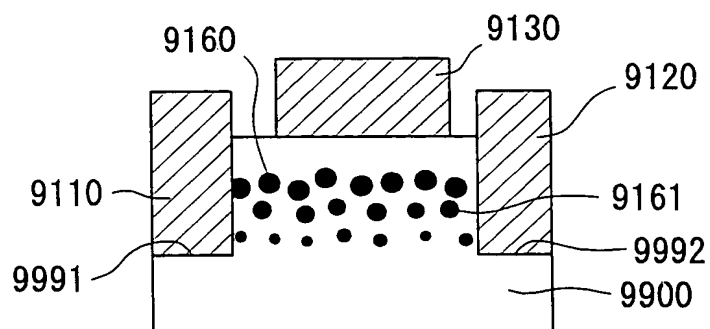
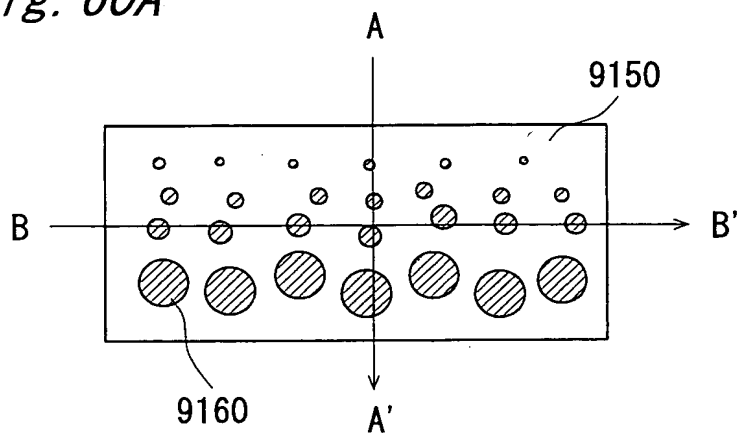
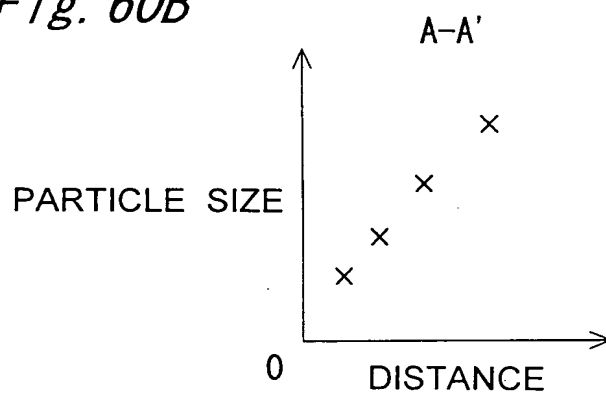
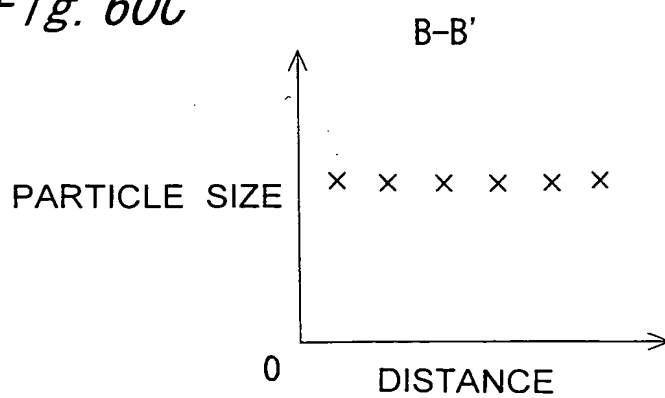


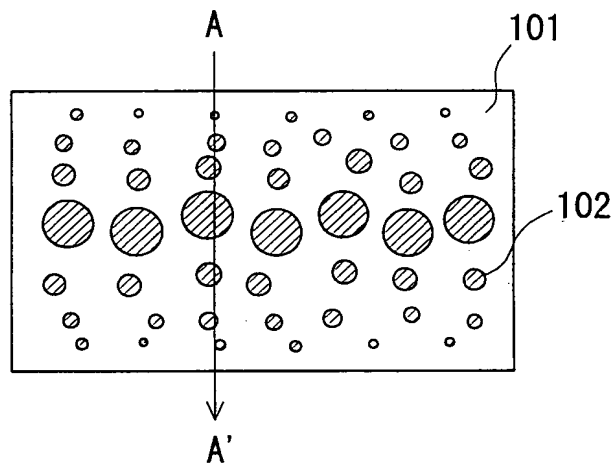
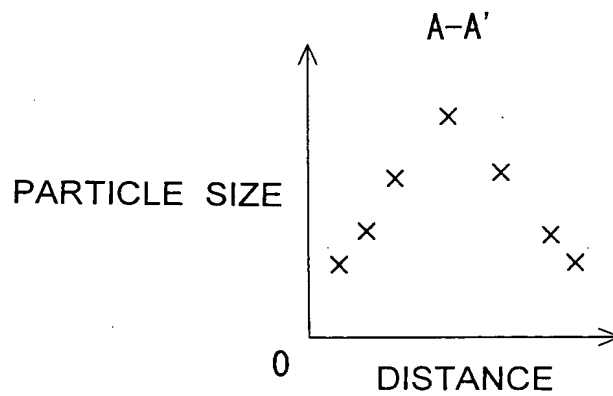
Fig. 59E



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*Fig. 60A**Fig. 60B**Fig. 60C*

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*Fig. 61A**Fig. 61B*

*Fig. 62*